United States Court of Appeals for the Federal Circuit

IN RE RAMBUS INC.

2011-1247

Appeal from the United States Patent and Trademark Office, Board of Patent Appeals and Interferences in Reexamination No. 90/010,420.

Decided: August 15, 2012

J. MICHAEL JAKES, Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, of Washington, DC, argued for appellant. On the brief was KATHLEEN A. DALEY, of New York, New York. Of counsel on the brief were PAUL M. ANDERSON, Paul M. Anderson, PLLC. of Austin, Texas; and RICHARD G. TARANTO, Farr & Taranto, of Washington, DC; and PETER A. DETRE, Munger, Tolles & Olson, LLP, of San Francisco, California; and FRED A. ROWLEY, JR. and JEFFREY Y. WU, Munger, Tolles & Olson, LLP, of Los Angeles, California.

THOMAS W. KRAUSE, Associate Solicitor, United States Patent and Trademark Office, of Alexandria, Virginia, argued for appellee. With him on the brief were RAYMOND T. CHEN, Solicitor, and BRIAN T. RACILLA, Associate Solicitor.

Before RADER, *Chief Judge*, LINN and DYK, *Circuit Judges*.

LINN, *Circuit Judge*.

Appellant Rambus Inc. ("Rambus") appeals a final decision of the United States Patent and Trademark Office ("PTO") Board of Patent Appeals and Interferences ("Board") in a reexamination in which claim 18 of Rambus's U.S. Patent No. 6,034,918 ("'918 Patent") was found invalid as anticipated. Because substantial evidence supports the PTO's determination that claim 18, as correctly construed reads on the "memory module" in the prior art iAPX 432 Interconnect Architecture Reference Manual published by Intel Corp. in 1982 ("iAPX Manual"), this court affirms.

I. BACKGROUND

A. The '918 Patent

The '918 patent is titled "Method of Operating a Memory Having a Variable Data Output Length and Programmable Register" and is one of a family of patents that claim priority to U.S. Patent Application No. 07/510,898 ("'898 Application"). The patents derived from the '898 Application collectively make up the "'898 family." The '898 Application has a priority date of April 18, 1990, and thus, the '918 Patent is now expired.

By the early 1990's, companies had begun developing synchronous memory devices and related technology. In contrast to the prior asynchronous memory devices, synchronous memory devices read and write data with reference to an external clock signal, allowing greater

control and faster data storage and retrieval. Previous memory devices would output all of the data located at a requested address, and that data would be filtered so only the desired data would be passed on to the processor. The '918 Patent describes a method where synchronous memory devices output only a specified amount of data in response to a request.

Claim 18 of the '918 Patent, at issue in this appeal, reads as follows:

> A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:
>
> receiving an external clock signal;
>
> receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request;
>
> receiving a first request from the bus controller; and
>
> outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to the external clock signal.

'918 Patent col. 26 ll. 13-27.

B. District Court Proceedings

In 2005, Rambus sued Hynix Semiconductor, Inc. ("Hynix") and several other chip manufacturers, including

Micron Technology, Inc. ("Micron") in the United States District Court for the Northern District of California alleging infringement of several patents in the '898 family. The district court consolidated the cases and considered the construction of the term "memory device." The district court initially construed "memory device" broadly as "a device in which information can be stored and retrieved electronically." *See* Order Clarifying the Court's Construction of "Memory Device" at 2 *Rambus Inc. v. Micron Tech., Inc.* ("*Micron*"), No. 06-cv-00244 (N.D. Cal. Nov. 21, 2008), ECF No. 1381 ("Micron Order").

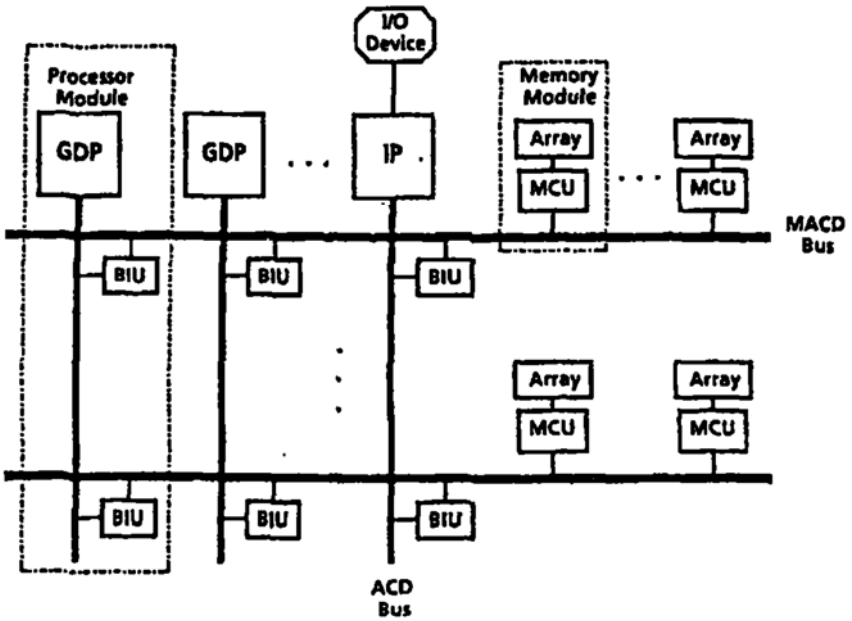
Rambus then explained to the court that defendants would seek to invalidate Rambus's patents based on prior art memory systems, and moved the court to reconsider its construction. The court clarified its construction of "memory device," explaining that while a memory device is not restricted to a single chip, it is limited "in scale to being a component in a memory subsystem." Micron Order at 2-3. With respect to the memory device's function, the district court noted that "memory devices" are distinct from "processing devices," but explained that a memory device is a "complete, independent memory subsystem with all the functionality of a prior art memory board in a conventional backplane-bus system." Micron Order at 3. Thus, the district court concluded that a "'memory device' does not include a microprocessor like a CPU or memory controller. It connects to a bus as a component in a larger system. While its size is not explicitly defined, it is on the order of a single chip, and smaller than a 'memory board.'" *Id.*

C. Reexamination Proceedings

In 2009, the district court entered final judgment finding that Hynix infringed claims 24 and 33 of the '918 patent. *See* Final Judgment, *Hynix Semiconductor, Inc. v.*

Rambus Inc., No. 00-cv-20905 (N.D. Cal. Mar. 10, 2009), ECF No. 3911 ("*Hynix*") (not discussing claim 18). Shortly thereafter Hynix sought *ex parte* reexamination of claims 18, 24, and 33 of the '918 Patent. During reexamination, the examiner construed the term "memory device" broadly as a "device[] that allows for the electronic storage and retrieval of information." *Ex parte Rambus, Inc.*, Reexamination No. 90/010,420, slip op. at 19 (B.P.A.I. Jan. 12, 2011) ("*Board Op.*"). Under this construction, the examiner found the '918 Patent's "memory device" analogous to the memory module disclosed in the iAPX Manual, which consists of a passive array of chips ("Array") and a memory control unit ("MCU"). The examiner confirmed claims 24 and 33, but with the iAPX memory module satisfying the memory device element, he rejected claim 18 as anticipated by the iAPX Manual.

Rambus appealed the examiner's rejection to the Board. On appeal, the Board defined the key issue as "whether the memory 'device' recited in claim 18 reads on the memory 'module' disclosed in the iAPX Manual." *Board Op.* at 3. Figure 1-2 from the iAPX Manual depicts the iAPX 432 Interconnect Topology as:



The Board then framed "[t]he central dispute [as] whether the claimed term 'device' is limited to a single 'chip' embodiment or also embraces a 'memory stick' [or transceiver device] embodiment as disclosed in the '918 patent." *Id.* Accordingly, the Board's analysis focused on the specification's teaching that "[i]n general, each teaching of this invention which refers to a memory device can be practiced using a transceiver device and one or more memory devices." '918 Patent col. 20 ll. 5-8. Rambus pointed to the prosecution history, specification, and expert declarations to support its contention that a skilled artisan would interpret a memory device as a single chip component.

The Board agreed with the district court in *Micron* that "claim 18 does not recite a chip device and the patentee must live with the broader memory device term recited." The Board also agreed that a memory device as used in the '918 Patent cannot be defined by the exact number of chips it is composed of—but that number does not have to be restricted to one. The Board also noted that the memory stick embodiment does not appear to have a CPU or microprocessor. The Board then cited to Rambus' expert declaration that the MCU in the iAPX Manual merely receives and translates instructions from the Bus Interface Unit ("BIU") and concluded that the MCU is not a microprocessor or CPU. Therefore, the Board equated the iAPX "memory module" with the '918 Patent's "memory device" and affirmed the examiner's rejection of claim 18 as anticipated by the iAPX Manual. Rambus timely appealed. This court has jurisdiction pursuant to 28 U.S.C. §1295(a)(4)(A).

II. Discussion

A. Standard of Review

Claim construction is a question of law that this court reviews de novo. *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1451 (Fed. Cir. 1998) (en banc). While claims are generally given their broadest possible scope during prosecution, *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000), the Board's review of the claims of an expired patent is similar to that of a district court's review, *Ex Parte Papst-Motoren*, 1 USPQ.2d 1655, 1655-56 (B.P.A.I. Dec. 23, 1986); *see also* MPEP § 2258 I.G (directing Examiners to construe claims pursuant to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), during reexamination of an expired patent).

Anticipation is a question of fact and we uphold the Board's factual determinations unless they are not supported by substantial evidence. *Hyatt*, 211 F.3d at 1371-72.

B. Claim Construction

The PTO contends that the Board correctly focused its analysis on construction of the term "memory device" in claim 18 of the '918 Patent and affirmed the examiner's rejection based on a construction of this term as meaning a "device[] that allows for the electronic storage and retrieval of information." *Board Op.* at 19. The Board also discussed the district court's construction of a "memory device" in *Micron*. The PTO argues that the Board supported these constructions by relying on the specification's description of a memory stick embodiment, the prosecution history, expert testimony, and language in Rambus's other patents.

Rambus, on the other hand, argues that the Board erred because a "memory device" has two relevant limitations: (1) it is a single chip component and (2) it does not have a memory controller. Rambus disputes the examiner's and Board's construction because the Board consid-

ered each word individually and then construed the phrase to cover "multiple electronic appliances grouped together, that allow[] information to be stored and retrieved." Appellant's Br. 21. According to Rambus, this broad construction makes no sense in the context of the '918 Patent. Instead, Rambus would define the term "memory device" as necessarily consisting of only one chip with no control function, and would not define the term by what its two component words individually mean. We consider each of the limitations Rambus suggests in turn.

1. Single Chip Limitation

Rambus relies on language from the specification, expert testimony, and the prosecution history of the '918 Patent to support its argument that a "memory device" must be a single chip device.

a. The Specification

Rambus points to portions of the specification where "memory device" refers to a single chip component. '918 Patent col. 17 ll. 14-27, col. 3 ll. 61-63. Rambus then cites *Lisle Corp. v. A.J. Manufacturing*, 298 F.3d 1306, 1314 (Fed. Cir. 2005), and argues that the stated goals of the invention could be achieved only through a single chip memory device. Finally, Rambus disagrees with the weight the Board afforded the "memory stick" embodiment disclosed in the specification. According to Rambus, the disclosure of the memory stick as an alternative to a memory device shows that they are two distinct embodiments.

The PTO concedes that the '918 Patent specification uses the term memory device to describe single chip embodiments of the invention, but stresses that nothing in the specification *limits* the invention to such devices. The PTO agrees with the Board that the multichip mem-

ory stick embodiment disclosed in the specification is an example of a memory device and posits that this embodiment proves these devices can consist of more than one chip.

This court agrees with the Board that the specification does not restrict the invention to single chip memory devices. There are no words of manifest exclusion or clear disavowals of multichip devices—there are only preferred embodiments and goals of the invention that Rambus argues are better met by single chip devices. The specification language Rambus cites shows only that the invention can be carried out with a single chip memory device, it does not require the invention to be so performed. '918 Patent col. 17 ll. 17-27 (referring to an embodiment where a single RAM supplies all bits for a block request). Other portions of the specification that Rambus cites are completely inapposite to the determination of the number of chips in a memory device. Rambus stresses that the invention allows "high-speed access to large blocks of data from a *single memory device*." Appellant's Br. 27 (emphasis in original). But this in no way indicates that the single memory device must be made of a single memory chip. Rambus has not demonstrated that a "memory device" is a term of art, and nothing indicates these other "devices" are limited to single chips. To the extent Rambus wanted to limit the memory device to a single chip component, it could have expressly done so. It did not, and this court will not do so here.

The Board's equating the multichip "memory stick" with a "memory device" to support its conclusion that the memory device is not limited to a single chip is, however, incorrect. The specification could not be clearer that the disclosed invention can be practiced with either a memory device or with a memory stick. '918 Patent col. 20 ll. 5-8. While the Board was incorrect that a memory device and

memory stick are the same, this does not mean that a memory device must contain only one chip.

b. Expert Testimony

Rambus cites testimony previously made on Hynix's behalf, which suggests a memory device is made of a single chip. Rambus also points to a joint-stipulation it previously made with Hynix during district court litigation. There the parties agreed that "memory device" in a related patent meant "an integrated circuit device in which information [could] be stored and retrieved electronically." Joint Claim Construction and Prehearing Statement at 1 *Hynix Semiconductor Inc. v. Rambus, Inc.*, No. 00-20905 (N.D. Ca.). This court previously construed "integrated circuit device" as a single chip. *Rambus v. Infineon Techs. Ag*, 318 F.3d 1081, 1091 (Fed. Cir. 2003). Thus, Rambus urges us to conclude that a skilled artisan would interpret "memory device" as a single chip component.

The PTO counters that claim 18 of the '918 Patent is directed to broad subject matter and "memory" is more accurately read as an adjective modifying "device." The PTO argues that the plain language of the claim does not restrict "memory devices" to single chip components and that the word "device" is broad enough to cover any component for carrying out the memory functions of a computer.

We agree with the PTO. With respect to the meaning of the term "memory device," the expert testimony on which Rambus relies directly conflicts with the testimony on which the Board relies. The Board cites to *Hynix* where Hynix's expert specifically described how a memory device might consist of more than one chip. In contrast, Rambus stresses the joint stipulation in *Hynix* where Hynix agreed to define a memory device as an integrated

circuit device, and Hynix's expert Desi Rhoden's ("Rhoden") unrelated interference testimony that a memory device is "typically not" a card with multiple memory chips on it. According to Rambus, these are instances where even its adversary recognized that a "memory device" is understood to be a single chip component. But Rhoden's testimony stated only that a card with multiple package memory chips on it is typically not a memory device. She did not say that a memory device must be made of a single chip. Ultimately, the expert testimony is conflicting and unpersuasive.

c. Prosecution History and Related Patents

Rambus argues that it distinguished U.S. Patent No. 4,315,308 ("Jackson") during prosecution of the '918 Patent based on the number of chips in a memory device. The PTO counters that the distinctions Rambus drew to overcome Jackson did not limit the term to a single chip. According to the PTO, Rambus distinguished Jackson on other grounds. The PTO is correct; Rambus distinguished Jackson during prosecution on the basis that the "memory device" of the '918 Patent did not perform the functions performed by Jackson's BIU—an argument we analyze in more detail, *infra*, in connection with the "memory controller" issue.

The PTO also asserts a claim differentiation argument, directing the court to other patents in the '898 family where Rambus used the term "memory device" in some claims but specifically claimed single chip components in others. The parties agree that "unless otherwise compelled . . . the same claim term in the same patent or related patents carries the same construed meaning." *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 (Fed. Cir. 2003). In related U.S. Patent No. 5,638,334 ("'334 Patent) independent claim 1 recites a "memory

device" while dependent claim 6 covers memory devices "formed on a single semiconductor substrate." *Compare* '334 Patent col. 25 ll. 2-17, *with* '334 Patent col. 26 ll. 1-2. Rambus argues that because dependent claim 6 adds the limitation that the substrate be a semiconductor, the word single does not necessarily limit the term "memory device," which, according to Rambus, already indicates a single chip. But if a memory device were always a single chip there would be no need to use the word "single" in claim 6, but not claim 1, regardless of any limitation regarding the substrate. Similarly, claim 1 of related U.S. Patent No. 5,954,804 ("'804 Patent") refers to a memory device, and claim 15 refers to an "integrated circuit device" with a "plurality of memory cells" (i.e., a single chip). *Compare* '804 Patent col. 24 l. 43, *with* '804 Patent col. 25 l. 62. *See also Infineon*, 318 F.3d at 1091; Appellant's Br. at 22.

In sum, "memory device" is a broad term which has been used consistently in the '918 patent and in the family of patents related to it to encompass a device having one or more chips. Moreover, and consistent with the district court's opinion in *Micron*, there is no basis to find a disavowal or redefinition that would limit the term "memory device" to a single chip.

2. Memory Controller

Rambus also disagrees with the examiner's construction of the term "memory device" as encompassing devices that perform a control function.

As an initial matter, the PTO contends that Rambus waived this argument because Rambus did not raise the issue in its appeal to the Board. *See In re Watts*, 354 F.3d 1362, 1367-68 (Fed. Cir. 2004). We disagree. Rambus did in fact raise this argument in its appeal brief before the Board, maintaining that the memory device in claim 18 of

the '918 Patent consists of a single memory chip and arguing that the examiner's construction was even broader than the district court's construction, which concluded that the memory device "does not include a microprocessor like a CPU or memory controller." Patent Owner's Appeal Br. at 15 *Ex parte Rambus, Inc.*, Reexamination No. 90/010,420 (May 4, 2010).

On the merits, Rambus argues that the term memory device cannot include a memory controller and cites *Lisle* to argue that the speed and efficiency goals of the invention described by the specification require that the memory devices be kept as simple as possible, thus excluding a memory controller. 298 F.3d at 1314. Rambus also points to portions of the specification indicating that control functions are carried out by master devices, not slave devices like the memory device. *See* '918 Patent col. 7 ll. 32-65 (fault tolerance), col. 16 ll. 54-56 (error checking), col. 14 ll. 38-44 (queuing requests), col. 14 ll. 59-67 (device configuration). According to Rambus, these time consuming control operations are carried out by the master devices and do not slow the transfer of data from the slave memory devices, which simply respond to signals. Rambus also argues that the term "memory device" cannot be construed to include a controller because Rambus's "argument for allowance [over Jackson] hinged on the BIU—a memory controller—*not* being part of the claimed memory device." Appellant's Br. 45 (emphasis in original).

The PTO disagrees with Rambus's master-slave analogy and instead argues that the specification makes clear that the '918 Patent's memory device includes functions like those performed by the iAPX manual's MCU. The PTO also agrees with the district court's conclusion that the memory device can, and indeed must, provide at least the control functionality necessary to enable the memory chip or chips to interface with the rest of the system, similar to how the MCU controls the array in the iAPX

Manual. The PTO argues this is true even if the argument to overcome Jackson resulted in a disclaimer of a CPU or global bus controller.

We agree with the PTO. Rambus's construction broadly excluding any memory controller that provides more functionality than simple control logic fails. First, claim 18 itself does not limit any "control" function that the memory device might carry out. In fact, the claim expressly calls for the memory device to provide the control functionality of receiving block size requests and outputting specific amounts of data. Nothing in the claim prevents the memory device from consisting of a storage chip and a device that facilitates the receiving and outputting from that storage chip. And at oral argument Rambus conceded that the memory device must at minimum have such control logic. *See* Oral Arg. at 12:20-12:33, *available at* http://www.cafc.uscourts.gov/oral-argument-recordings/2011-1247/all. Rambus only attempted to exclude more complex controllers from the memory device. Oral Arg. at 15:35-15:50. But excluding more complex controllers does not eliminate all control functionality.

Nor does *Lisle* compel a different result. In *Lisle*, "an object of the patented invention [was] to provide a single tool that [could] be used on many different tie rod configurations." 398 F.3d at 1314. That goal informed the construction of a claim limitation because a contrary construction would have rendered the invention mechanically incapable of meeting that goal. *Id.* Here, the general speed and efficiency goals Rambus relies on do not require a construction of "memory device" that excludes all control functionality. Pursuant to claim 18, the memory device needs only to receive and output specific data, functions it can perform even while exhibiting other minor functionality, without wholly defeating the invention's speed and efficiency goals. And while Rambus did

exclude the functions of Jackson's BIU during prosecution, this restriction only prevents the memory device from containing a global bus controller or CPU, not from containing a component that interfaces with the computer system, even when that component provides some additional functionality.

Finally, Rambus admits that a key part of the '918 Patent's invention was a device with "'all the functionality' of prior art memory boards." Appellant's Br. 39. Thus, a memory device is not just a functionless storage chip. The memory device must have some functionality—specifically the data receiving and outputting functions described in claim 18. Thus, consistent with the specification, prosecution history, and the *Micron* district court's construction, we construe a "memory device" as a component of a memory subsystem, not limited to a single chip, where the device may have a controller that, at least, provides the logic necessary to receive and output specific data, but does not perform the control function of a CPU or bus controller.

B. Anticipation

The parties entire anticipation dispute turns on whether the memory device in claim 18 of the '918 Patent reads on the memory module in the iAPX Manual. We conclude that substantial evidence supports the Board's decision that it does.

The Board accepted Rambus's characterization of the iAPX Manual's module as "contain[ing] at least 12 TTL packaged chips, a memory controller chip, and several DRAM chips" without further comment on the examiner's control function analysis. *Board Op.* at 12. Correctly construed, the "memory device" described in claim 18 of the '918 Patent can contain more than one chip and may contain a controller that provides the logic necessary for

the memory device to receive and output specific data, but that controller does not function like a CPU. Rambus agreed at oral argument that the MCU in the memory module of the iAPX Manual provided the necessary logic, but tried to distinguish the MCU because it "does more than that." Oral Arg. at 15:22-15:35. But as the examiner recognized, it is the bus controller (i.e., the "BIU") of the iAPX that is akin to the BIU that Rambus distinguished during prosecution, not the local "MCU" that is within iAPX's "memory module." There is no suggestion that the BIU of the iAPX is within the memory module, rather it is clearly outside of the memory module, thus satisfying the requirement that the memory module receive a request from a bus controller. By not restricting a memory device to a single chip or otherwise restricting the necessary interface control logic function within the claims, there is simply no principled way to distinguish the iAPX Manual's memory module, which contains several chips and a controller that provides the logic for those chips to function, from the '918 Patent's memory device. Thus, substantial evidence supports the Board's conclusion that the iAPX memory module reads directly on the '918 Patent's memory device.

III. CONCLUSION

For the foregoing reasons, this court affirms the Board's rejection of claim 18 of the '918 Patent as anticipated by the iAPX Manual.

AFFIRMED