NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

PROMOS TECHNOLOGIES, INC.,
Appellant

v.

SAMSUNG ELECTRONICS CO., LTD.,
Appellee

2019-1343

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01412.

PROMOS TECHNOLOGIES, INC.,
Appellant

v.

SAMSUNG ELECTRONICS CO., LTD.,
Appellee

2019-1344

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01413.

Decided: April 6, 2020

KEVIN CHRISTOPHER JONES, TechKnowledge Law Group LLP, Redwood City, CA, argued for appellant. Also represented by CRAIG R. KAUFMAN.

NAVEEN MODI, Paul Hastings LLP, Washington, DC, argued for appellee. Also represented by CHETAN BANSAL, STEPHEN BLAKE KINNAIRD, JOSEPH PALYS.

Before O'MALLEY, REYNA, and WALLACH, *Circuit Judges*.

Opinion for the court filed by *Circuit Judge* O'MALLEY.

Dissenting opinion filed by *Circuit Judge* REYNA.

O'MALLEY, *Circuit Judge*.

In two inter partes review proceedings requested by Samsung Electronics Co. ("Samsung"), the U.S. Patent Trial and Appeal Board ("the Board") invalidated all challenged claims of U.S. Patent No. 6,069,507 (the "'507 patent"), which is assigned to ProMOS Technologies, Inc. ("ProMOS"). J.A. 3; J.A.II. 3. [1] The Board found the challenged claims unpatentable as anticipated and obvious.

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[1] This opinion primarily cites to the briefing and appendix from the -1343 appeal because the briefing and appendices for the two appeals are substantially identical on the claim construction issue. Any citations to the -1344 briefing and appendices will use the modifier "II," *e.g.*, "J.A.II.," "Appellant Br. II," "Appellee Br. II"

ProMOS appeals the Board's final written decisions, arguing that the Board's invalidity findings are erroneous because its construction of the "maintaining" limitation is erroneous. Because we agree with the Board's construction, we *affirm* the Board's decisions.

I. BACKGROUND

A. The Technology

A clock signal is a type of periodic signal that oscillates between low and high voltages, and is often used to coordinate or synchronize different parts of a circuit. J.A. 227. The most common type of clock signal is in the form of a square wave, usually with a fixed, constant frequency:

J.A. 227. The period (or cycle) of a clock signal is the duration between one LOW-to-HIGH transition, also called a "rising edge," and the next LOW-to-HIGH transition. J.A. 227. The HIGH-to-LOW transition is similarly called a "falling edge." One period of a clock signal spans a 360° phase. J.A. 228. When the rising and falling edges of two clock signals do not occur at the same time, the two signals are not "phase-aligned." J.A. 228. This difference is known as a "phase difference."

One challenge associated with digital circuits is "clock skew"—that is, when a clock signal originating from a given source arrives at different components in a circuit at different times. J.A. 229–30. Clock skew may be caused by a variety of spatial or physical conditions, *e.g.*, differing lengths of wire for conducting clock signals to respective components. J.A. 230. When circuit components have different perceptions of timing due to clock skew, this may lead to undesirable circuit behavior. J.A. 230. For example, if two circuit components—which are designed to

execute actions simultaneously—receive copies of a clock signal that are not phase-aligned due to clock skew, the actions will occur sequentially.

One way to address this issue is through a system known as a "delay locked loop" ("DLL"). A DLL, via a "phase detector," determines how much of a phase difference there is between two clock signals: a reference (or input) clock and an output (or feedback) clock. The DLL then employs a "voltage variable delay line" to delay the input data until it is synchronized with the reference clock.

B. The '507 Patent

The '507 patent, entitled "Circuit and Method for Reducing Delay Line Length in Delay-Locked Loops," relates to DLLs and "more particularly to reducing delay line length in DLLs." '507 patent, col. 1 ll. 12–13. Figure 1 of the patent provides an example of a "typical digital DLL" at the time of the invention.

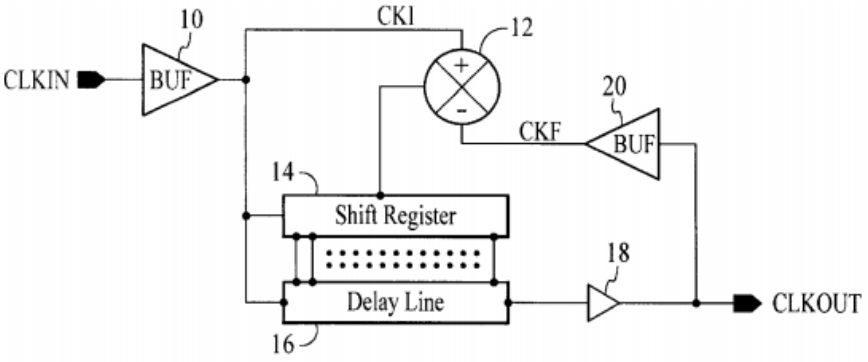

FIG. 1
(PRIOR ART)

In this "typical digital DLL," a phase detector 12 determines if a phase difference exists between the buffered input and feedback clock signals, "CKI" and "CKF." '507 patent, col. 1 ll. 19–33. If there is a nonzero phase difference between the two signals, the system shifts the

buffered input clock signal by adjusting the shift register 14 to select sufficient delay through delay line 16. '507 patent, col. 1 ll. 29–33. This added delay synchronizes the input and feedback clock signals. *Id.*

Although DLLs can resolve the problems associated with clock skew, they generally require long delay lines to achieve sufficient coverage of frequency ranges and guarantee desired resolution. '507 patent, col. 1 ll. 16–18. This increased delay line length may demand larger silicon area requirements and higher power consumption. '507 patent, col. 1 ll. 42–44. Increased delay line length may also cause other problems, such as a longer lock-in time and greater high frequency signal distortion. '507 patent, col. 1 ll. 44–46.

The '507 patent proposes a "more elegant and cost effective" solution for reducing delay line length in a DLL. Figure 2, the only embodiment described in the written description, illustrates a "digital DLL 24 in accordance with the present invention." '507 patent, col. 2 ll. 49–50.

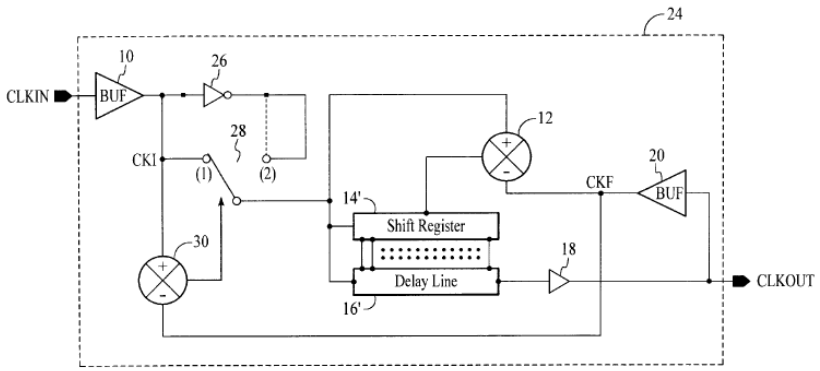

FIG. 2

The DLL 24 has an additional phase detector 30, which determines a phase difference between the buffered input clock signal CKI and a feedback clock signal CKF. '507 patent, col. 2 ll. 61–67. If the second phase detector 30

determines that the difference between the feedback clock signal CKF and the buffered input clock signal CKI is within a 180˚ phase difference, the second phase detector controls the switch 28 to be at position (1), as seen above. Under this configuration, clock signal CKI is provided as an input to the delay line 16. '507 patent, col. 2 l. 61–col. 3, l. 6. But if the phase difference between the two clock signals is greater than 180˚, the second phase detector controls switch 28 to be at position (2). Under this new configuration, the clock signal CKI is inverted by inverter 26 and then provided as an input to the delay line. '507 patent, col. 3 ll. 8–15. "Through the inversion, the phase difference needing to be compensated by the delay line 16' is made less than 180˚" which decreases the length of the delay line by "approximately one-half the length that a typical DLL would require for comparable clock deskewing needs." '507 patent, col. 3 ll. 11–18.

Independent claim 10 recites:

> A method for reducing delay line length in a digital delay locked loop (DLL), the method comprising:
>
> > determining a phase difference between an input clock signal and a feedback clock signal;
> >
> > maintaining the phase difference between the input clock signal and the feedback clock signal [within[2]] approximately 180˚,

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[2] Both the Board and the parties agree that the word "within" is missing from the "maintaining" limitation and neither party challenged the Board's decision to read the claim to include "within." J.A. 7. During prosecution, the applicant amended the language of what became claim 10 to include, *inter* alia, the limitation "within approximately 180˚." J.A. 7. In addition, the examiner acknowledged that

> including adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line when the determined phase difference is less than approximately 180°; and
>
> delaying the input clock signal to compensate for the phase difference, wherein a number of delay cells utilized is reduced by approximately one-half.

'507 patent, col. 4 ll. 47–59.

Dependent claim 11 recites:

> The method of claim 10 wherein the phase detector comprises a phase difference detector with a first resolution.

'507 patent, col. 4 ll. 60–61.

C. The Prior Art

1. Donnelly (U.S. Patent No. 5,945,862)

Donnelly, a U.S. patent entitled, "Circuitry for the Delay Adjustment of a Clock Signal," relates to providing "adjustable delays" to an incoming periodic signal, like a clock signal. J.A. 451. Donnelly discloses a DLL system. J.A. 453, col. 5 ll. 32–34. The DLL system determines a phase difference between an input clock signal and a feedback clock signal via its phase detector. Donnelly explains that the DLL operates as follows: (1) the phase detector detects a nonzero difference between the two clock signals and instructs a counter to determine this difference; (2) the circuit block receives information which instructs the selector to switch consecutively through the taps from the output of the blender circuit to reduce the phase error; and (3) the

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the maintaining step recites "within approximately 180 degree[s]." J.A. 7.

selector switches consecutively through the taps until it eliminates the phase difference. J.A. 453, col. 5 l. 39–col. 6 l. 1. Donnelly explains that this process of constantly adjusting the value in the counter causes the output signal to "jitter" around the desired phase relationship between the input clock signal and the feedback clock signal. J.A. 453, col. 6 ll. 1–8.

2. Kim (U.S. Patent No. 5,875,219)

Kim, a U.S. patent entitled "Phase Delay Correction Apparatus," discloses a digital DLL with an improved phase delay correction apparatus. J.A.II. 668, col. 1 ll. 5–10. The DLL includes a phase detector for outputting a comparing signal, a shift register that can sequentially shift data bit values in both directions in accordance with the comparing signal, a phase delay unit for delaying and outputting the system clock signal, a domain selecting controller, and a domain selector for adjusting the phase of a driving signal from one region comprising approximately 0–180˚ to another area comprising approximately 180–360˚. J.A.II. 668, col 2 ll. 38–64.

D. The Board's Decisions

As relevant to this appeal, Samsung filed two IPR petitions asserting that claims 10 and 11 of the '507 patent are unpatentable because they would have been obvious in view of Donnelly and Iwamoto (U.S. Patent No. 5,875,219)[3] and are anticipated by Kim. J.A. 133; J.A.II. 115. In its petitions, Samsung asserted that Donnelly and Kim disclose "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180˚" (the "maintaining limitation"), as required by claim 10. J.A. 157–187; J.A.II. 129–55. Samsung and its expert, Dr. R. Jacob Baker, explained that the input and

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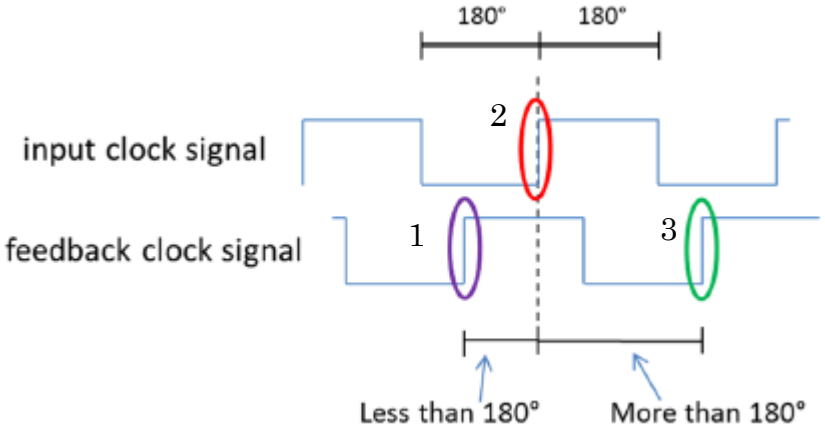
[3] The disclosures of Iwamoto are not relevant to this appeal.

feedback clocks in Donnelly and Kim have the same frequency and the same period. Under this assumption, the clock signals disclosed in the two references "always have a phase difference within 180˚." J.A. 277–80; J.A.II. 217–27. To illustrate Samsung's point, Dr. Baker offered the following example:



J.A. 279 (annotated). The figure above shows two clock signals, an input clock signal and a feedback clock signal, with the same frequency and period. In this example, the later rising edge of the feedback clock signal (3) lags behind the rising edge of the input clock signal (2) by more than 180˚. The phase difference between the two signals is more than 180˚. But the earlier rising edge of the feedback clock signal (1) is less than 180˚ ahead of the same rising edge of the input clock signal (2). The phase difference between these two signals is within approximately 180˚. Therefore, regardless of how the feedback clock signal is shifted, a rising edge of the feedback clock signal will always be within approximately 180˚ of the input clock signal. J.A. 279.

In its Patent Owner Preliminary Responses, ProMOS did not dispute that a feedback clock signal is always within either 180˚ ahead or 180˚ behind an input clock signal with the same period and frequency. Instead, ProMOS

argued that the "maintaining" limitation should be construed as meaning "ensuring that the feedback clock signal ***follows behind*** the input clock signal by less than 180°." J.A. 833 (emphases added). ProMOS asserted that a reading of the limitation that covered a variation in either direction is inconsistent with the intrinsic record and would, in effect, render the limitation meaningless. J.A. 831–33.

In its Institution Decisions, the Board agreed with ProMOS's construction of the "maintaining" limitation. J.A. 867–69. The Board accepted ProMOS's characterization of the prosecution history and agreed with ProMOS that Samsung's interpretation would render the claim term "meaningless." J.A. 867–69. Accordingly, the Board initially did not institute IPRs on challenged claims 10 and 11, but instituted the IPRs based on other unpatentability grounds, involving other claims (claims 13 and 15) that are not at issue in this appeal. J.A. 892–93.

After the Supreme Court's decision in *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348 (2018), the Board issued orders in both IPRs, instituting on claims 10 and 11. J.A. 1042–43. Due to the limited scope of the original institution, however, ProMOS's Patent Owner Responses only addressed claims 13 and 15. Accordingly, the Board asked the parties if further briefing was necessary for claims 10 and 11. J.A. 1042–43. In response, ProMOS "indicated that it has nothing to add, for claims 10 and 11, and would be satisfied if [it] could simply rely on arguments made in [the] Patent Owner's Preliminary Response for claims 10 and 11." J.A. 1047–48. Samsung, however, requested that it be allowed to file replies that addressed the arguments for claims 10 and 11 in ProMOS's Preliminary Responses. J.A. 1048. The Board granted Samsung's request. J.A. 1048–49.

In its reply, Samsung argued that the Board should adopt the plain and ordinary meaning of the "maintaining" limitation—one without a directionality requirement—because the claim language, specification, and prosecution

history cut against ProMOS's proposed construction. J.A. 1074–85. Samsung argued that: (1) there was no "clear and unmistakable disavowal" of the full scope of the "maintaining" limitation; (2) the specification and the language of claim 13 demonstrated that the patent applicant deliberately chose not to inject a directionality requirement into the "maintaining" limitation; and (3) as confirmed by ProMOS's own declarant, the specification itself does not support ProMOS's construction. J.A. 1074–80. Samsung explained that the sole embodiment describes a phase difference between the input and feedback clock signals that oscillates between less than 180° and more than 180°. J.A. 1080–83. Samsung also pointed out that ProMOS's Preliminary Response had misrepresented the prosecution history that had led the Board to originally deny institution on claims 10 and 11. J.A. 1083–85.

The Board rejected ProMOS's proposed construction of the "maintaining" limitation the second time around. In its Final Written Decisions, the Board stated that it had changed its mind after reviewing "the complete trial record," noting that the intrinsic evidence supported a finding that the limitation imposes no directionality requirement, such that one signal must follow the other by within approximately 180°. J.A. 16–22. In particular, the Board explained that ProMOS's interpretation of the prosecution history was "internally inconsistent and self-contradictory," and found no disavowal by the applicant with regard to the subject matter of claim 10. J.A. 19–21. The Board concluded that the "maintaining" limitation "imposes no directional [sic] requirement, so either signal can be ahead or behind the other by within approximately 180°." J.A. 22. Based on this construction, the Board determined that Donnelly and Kim both disclose the "maintaining" limitation. J.A. 40–45; J.A.II 32–38. The Board found that Samsung had established, by a preponderance of the evidence, that the challenged claims are anticipated by Kim and

would have been obvious over the combined teachings of Donnelly and Iwamoto. J.A. 45

ProMOS timely appealed the Board's final decisions. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

II. DISCUSSION

ProMOS appeals: (1) the Board's construction of the "maintaining" limitation; and (2) the Board's anticipation and obviousness findings based on its construction of the "maintaining" limitation. Both parties agree that the claim construction dispute is dispositive to the Board's anticipation and obviousness findings. Appellant Br. 10 ("Claim construction is dispositive in this appeal."); Appellee Br. 38 ("It is undisputed that if the Board's construction is upheld, then there can be no error in the Board's finding of unpatentability."); Appellant Reply Br. 9. Accordingly, we address the claim construction dispute inquiry first.

A. Claim Construction

This court reviews the ultimate construction of a claim de novo. *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318 (2015). The court reviews subsidiary factual findings for substantial evidence. *Knowles Elecs. LLC v. Iancu*, 886 F.3d 1369, 1374 (Fed. Cir. 2018). When we review the claim construction of a patent term in an IPR appeal after the patent has expired, such as in this case, we apply the standard established in *Phillips*, not the "broadest reasonable interpretation." *See In re CSB-Sys. Int'l, Inc.*, 832 F.3d 1335, 1342 (Fed. Cir. 2016). That is, the words of a claim "are generally given their ordinary and customary meaning," as the term would have been understood by a person of ordinary skill in the art at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005).

ProMOS argues that the Board's construction of the "maintaining" limitation is erroneous because it does not include a directionality requirement. According to

ProMOS, the "maintaining" limitation should be construed as "ensuring that the feedback clock signal *follows behind* the input clock signal by less than 180°." Appellant Br. 11 (emphasis added). In support of this argument, ProMOS relies on certain language from the written description and the prosecution history. As described in further detail below, however, ProMOS misinterprets the intrinsic evidence and attempts to import the narrower characteristics of an embodiment into an unrelated claim term.

1. The Plain Language of the Claims and the Written Description Do Not Support Importing a Directionality Restriction into the "Maintaining" Limitation

The plain text of the claim does not place a directionality restriction on the "maintaining" limitation. Claims 8 and 10, the only two claims reciting the limitation, simply require that the phase difference between the input and the feedback clock signals is maintained within 180°. '507 patent, col. 4 ll. 51–53 ("maintaining the phase difference between the input signal and the feedback clock signal [within] approximately 180°"). Neither claim states or implies that the phase difference between the two signals is calculated by how much the feedback signal "follows" or lags behind the input signal. '507 patent, col. 4 ll. 33–39, 51–53. Accordingly, unless "the patentee has chosen to be his own lexicographer in the specification or has clearly disclaimed coverage during prosecution," we must interpret claims according to their plain language. *See E-Pass Techs., Inc. v. 3Com Corp.*, 343 F.3d 1364, 1370 Fed. Cir. 2003). But there is no such explicit definition or disclaimer. Outside of claims 8 and 10, the '507 patent only refers to the "maintaining" limitation in two instances: in the Abstract and in the Summary of the Invention. '507 patent, Abstract; '507 patent, col. 2 ll. 3–11. In both cases, the limitation is described broadly, without a directionality modifier such as "behind." *Id.*

ProMOS argues that one of the statements in the written description, "CKF is more than 180° behind CKI," indicates that the "maintaining" limitation calculates the phase difference based on how much the feedback signal lags the input signal. Appellant Br. 12. The written description, however, supports no such inference. In discussing the sole embodiment, depicted in Figure 2, the '507 patent recites:

> When the second phase detector 30 determines that CKF [the feedback clock signal] is more than 180° behind CKI [the input clock signal], the second phase detector 30 controls switch 28 to be at position (2). The inverted buffered clock signal is thus selected, so that the input clock signal CKI is reversed by 180°[.] Through the inversion, the phase difference needing to be compensated by the delay line 16' is made less than 180° and within the normal operation capabilities of the phase adjusting loop formed by phase detector 12, shift register 14', and delay line 16'.

'507 patent, col. 3 ll. 7–15. This discussion of the preferred embodiment does not address the "maintaining" limitation. This passage explains that the phase detector "select[s]" the inverted buffered clock signal when it "determines" that the feedback signal is more than 180° behind the input signal. '507 patent, col. 3 ll. 7–15. It does not state that this directionality requirement should also apply when the DLL is "maintaining" the phase difference between the two signals. '507 patent, col. 3 ll. 7–15.

ProMOS conflates the "determining" and "selecting" steps with the separate "maintaining" limitation. As disclosed in claims 8 and 10 of the patent, the "maintaining" limitation does not involve "determining" whether a phase difference exists or "selecting" an inverted buffered clock signal. Read plainly, the claim language states that the DLL maintains the phase difference between the two

signals within approximately 180° by adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line when the determined phase difference is less than approximately 180°. '507 patent, col. 4 ll. 51–57. We need not construe the "maintaining" limitation so narrowly simply because an embodiment describes other steps, namely, the "determining" and "selecting" steps, which *do* have directional restrictions. In fact, this directionality restriction is captured by claim 13 of the '507 patent, which includes the "determining" and "selecting" limitations:

> A method for reducing delay line length in a digital delay locked loop (DLL), the method comprising:
>
> *determining* whether a feedback clock signal in the DLL *follows* within a 180° phase difference *behind* an input clock signal; and
>
> *selecting* a switch position according to the determining step, including selecting a first switch position when the feedback clock signal *follows behind* the input clock signal with 180°.

'507 patent, col. 4 l. 66–col. 5 l. 10 (emphases added). Like the discussion of the preferred embodiment, claim 13 acknowledges that these two steps include a directionality restriction. If the patentee wanted to import that same restriction—"follows behind"—into the "maintaining" limitation of claim 10, he could have used similar language. But he did not. The written description further confirms that the patentee understood how to describe the relationship between two clock signals in a manner that makes clear which clock signal leads or lags the other in phase. '507 patent, col. 2, ll. 63–66 ("When the second phase detector 30 determines that the feedback clock signal CKF from the DLL 24 is behind the buffered input clock CKI within a 180° phase difference . . . ."). We decline to adopt a narrower construction in contravention of the plain language of the claims.

And, even if we were to determine that the above passage pertains to the "maintaining" limitation, it is well established that claims may be broader than described embodiments. *See, e.g.*, *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1370 (Fed. Cir. 2008).

2. The Prosecution History Does Not Support ProMOS's Narrower Proposed Construction of the "Maintaining" Limitation

ProMOS argues that the examiner allowed claim 10 over Butcher (U.S. Patent No. 4,789,996), another prior art reference, because Butcher did not teach "maintaining the phase difference between the input clock signal and the feedback signal within 180 degrees." Appellant Br. 13 (citing J.A. 393). According to ProMOS, "Butcher teaches a phase locked loop having input and feedback clock signals with equal frequencies." *Id.* ProMOS insists that, if the examiner had understood the "maintaining" limitation under the Board's construction, "he could not have reached the conclusion he did—that the DLL in Butcher did not teach the claimed 'maintaining' step." *Id.*

ProMOS's argument requires several logical leaps. In order to arrive at the same conclusion as ProMOS, the record must establish that: (1) the input and feedback clock signals disclosed in Butcher have the same frequencies; (2) the examiner knew that these clock signals have equivalent frequencies; and (3) the examiner's allowance of the "maintaining" limitation was directed to the "within 180°" part of the maintaining step, and not to the overall step itself. But whether the record supports these factual hurdles is irrelevant because ProMOS mischaracterizes the prosecution history. The patentee did not add the "maintaining" limitation to claim 10 in order to overcome rejection.

During prosecution, the examiner rejected pending claim 8, which included the "maintaining" limitation, as obvious in view of Butcher. J.A. 393. Although the examiner

admitted that Butcher did not disclose the "maintaining" limitation, he concluded that the step would have been obvious to a person of ordinary skill in the art. J.A. 393 ("It would have been obvious to one skilled in the art to maintain a delay of 180 degrees by selecting a proper number of registers without changing the scope of the Butcher reference."). Pending claims 9 and 11 (now claim 10), which depended from pending claim 8 and had *additional limitations* on top of the "maintaining" limitation, were found to include allowable subject matter. J.A. 394. Accordingly, the patentee rewrote claims 9 and 11 in independent form, incorporating the features of claim 8 from which they depended. J.A. 406–07.

The record is clear: the "maintaining" limitation was not added to pending claim 11/now claim 10 in order to overcome the prior art, as argued by ProMOS. J.A. 33–34. Pending claim 11 already included the "maintaining" limitation based on its dependency on pending claim 8. These facts do not imply that the examiner somehow interpreted the "maintaining" limitation to include a directionality restriction, as ProMOS contends.

3. The Board's Construction Does Not Render the "Maintaining" Limitation Superfluous

Finally, ProMOS argues that the Board's construction of the "maintaining" limitation renders the limitation superfluous. Appellant Br. 16. Under the Board's construction, any two clock signals with identical frequencies (and therefore, identical periods) are always "within 180° of each other." ProMOS concludes that the limitation has "no real meaning" under this construction because the limitation is always satisfied.

The Supreme Court has stated that "[e]ach element contained in a patent claim is deemed material to defining the scope of the patented invention." *Warner-Jenkinson Co., Inc. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 29 (1997). Consistent with this philosophy, we have determined that

it is generally improper to construe a patent claim so that express claim limitations or elements are rendered superfluous. *See Biocon, Inc. v. Straumann Co.*, 441 F.3d 945, 950–52 (Fed. Cir. 2006). The distinction here, however, is that claims 8 and 10 of the '507 patent are not necessarily rendered "superfluous" by the Board's construction.

The plain language of the claims does not require the input clock signal and the feedback clock signal to have the same frequency and period. J.A. 131 at 4:47–59. Therefore, the Board's construction does not render the claimed maintaining step superfluous because a pair of clock signals with different frequencies would not satisfy the limitation. These facts are distinct from those present in our "superfluous" precedent, where the erroneous claim construction ignored the ordinary meaning of explicit claim limitations or read out limitations in their entirety. *See, e.g.*, *Biocon*, 441 F.3d at 950–52 ("In sum, the effect of adopting Diro's proposed claim construction would be to read limitations [a], [b], [e], and [h] out of the claim. Not only would that be contrary to the principle that claim language should not be treated as meaningless, but it would be contrary to the specification, which describes the features of the claimed abutment in detail . . . ."); *Elektra Instrument S.A. v. O.U.R. Sci. Int'l, Inc.*, 214 F.3d 1302, 1307 (Fed. Cir. 2000) (claim language "only within a zone extending between latitudes 30°–45°" does not read on a device with radiation sources extending between 14°–43° because "[a]ny other conclusion renders the reference to 30 degrees superfluous").

ProMOS contends that a DLL, such as the one disclosed in the '507 patent, always has clock signals with the same frequency because it is a necessary characteristic of a DLL circuit. Appellant Br. 16–17. But neither party presented evidence on this issue. J.A. 21–22 ("Patent Owner has not, either in its Preliminary Response or its Patent Owner Response, asserted in a DLL the input clock signal and the feedback clock signal necessarily would have the

same frequency. Petitioner has not had a full opportunity to respond to this new argument. Accordingly, the new argument, raised for the first time in Patent Owner's Sur-Reply, will not be considered."). ProMOS relies on deposition testimony from Samsung's expert stating that, "in the engineering sense," two synchronized DLL clock signals have the same frequencies and the same signals. J.A. 959 at 9:12–22. This, however, is not an admission that DLL clock signals always have the same input and feedback signals. In that context, Samsung's expert may have been defining "synchronization" instead of opining on the fundamental characteristics of clock signals in DLL circuits. We decline to adopt ProMOS's proposed construction without any supporting evidence in the record.

B. The Board's Unpatentability Determinations

Both parties agree that the claim construction dispute over the "maintaining" limitation is dispositive to the Board's anticipation and obviousness findings. Appellant Br. 10 ("Claim construction is dispositive in this appeal."); Appellee Br. 38 ("It is undisputed that if the Board's construction is upheld, then there can be no error in the Board's finding of unpatentability."); Appellant Reply Br. 9. Accordingly, because the Board correctly construed the "maintaining" limitation, we conclude that there is no error in the Board's findings of unpatentability.

III. CONCLUSION

The Board correctly construed the "maintaining" limitation. As both parties agree that our determination with respect to the Board's construction of that limitation is dispositive as to whether substantial evidence supports the Board's anticipation and obviousness findings, we affirm the Board's decisions in both IPRs.

AFFIRMED

COSTS

No costs.

NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

PROMOS TECHNOLOGIES, INC.,
Appellant

v.

SAMSUNG ELECTRONICS CO., LTD.,
Appellee

2019-1343

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01412.

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2019-1344

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01413.

REYNA, *Circuit Judge,* dissenting.

The '507 patent concerns an improvement to the operation of a delay locked loop—a circuit used to synchronize digital clocks by delaying the signal of one clock (here, an input clock signal) relative to the signal of another (here, a feedback clock signal) to compensate for the "phase difference" between the signals. At issue is whether this "phase difference," as used in the claim term "*maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°*" is to be measured in only one direction, i.e., as the lag of the feedback signal behind the input signal, or whether "phase difference" refers to the variance between the clock signals in either direction, i.e. as either the lag or the lead of the input signal relative to the feedback signal.

A careful analysis of the way "phase difference" is used in the claims, and the way the invention is described in the specification, makes clear that the phase difference recited in the '507 patent is unidirectional. Neither the majority nor the Board, however, engage in this analysis. Instead, they begin with the assumption that the "plain meaning" of the term "phase difference" is bi-directional. Only then do they turn to the intrinsic evidence to assess whether a "directional limitation" should be "imported" into the claims under the exacting criteria for lexicography and express disavowal.

This is contrary to the framework we set forth in *Phillips*, which dictates that the relevant plain meaning of a claim term is its meaning in the context of the patent, to be discerned at the outset in the context of the specification and other intrinsic evidence. Because the majority

embraces a construction of "phase difference" divorced from its usage in the patent and affirms the invalidation of the challenged claims based on that erroneous construction, I respectfully dissent.

I

It is well-established that we generally give claim terms their plain and ordinary meaning to a skilled artisan when read in the context of the specification and prosecution history. *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315-17 (Fed. Cir. 2005). The doctrines of lexicography and disavowal are narrow exceptions to this rule that are applied when we limit claim scope in contradiction to the claim language. *Thorner*, 669 F.3d at 1365 (citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1580 (Fed. Cir. 1996)).

The intrinsic evidence is therefore integral at the outset of claim construction for discerning the plain and ordinary meaning of claim terms in the context of the patent. *See Lexion Med., LLC v. Northgate Techs., Inc.*, 641 F.3d 1352, 1356 (Fed. Cir. 2011). ("The customary meaning of a claim term is not determined in a vacuum and should be harmonized . . . with the intrinsic record, as understood within the technological field of the invention."); *Abbott Labs. v. Andrx Pharms., Inc.*, 452 F.3d 1331, 1336 (Fed. Cir. 2006) ("Where claim terms are ambiguous or disputed, then we turn to the specification as . . . the single best guide to the meaning of a disputed term") (quoting *Phillips*, 415 F.3d at 1315)). In *Phillips*, we specifically cautioned against construing claims by first developing a broad definition of claim terms divorced from the context of the patent and then turning to the specification only to look for grounds for limiting the claim scope. *Phillips*, 415 F.3d at 1320 (discussing *Texas Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002)). Such an approach, we noted, posed a "risk of systematic overbreadth," which "is

greatly reduced if the court instead focuses at the outset on how the patentee used the claim term in the claims, specification, and prosecution history, rather than starting with a broad definition and whittling it down." *Id.* at 1321.

Thus, we have rejected a proposed claim construction where it relies on an initial "assumption" that a claim term has a broad "ordinary meaning" unsupported by the intrinsic or extrinsic evidence. *Ruckus Wireless, Inc. v. Innovative Wireless Sols., LLC*, 824 F.3d 999, 1003 (Fed. Cir. 2016). When the plain meaning of a claim term does not clarify whether and how a restriction applies, we have said that such ambiguity is to be resolved in the first instance by reviewing the claim language as a whole, the other intrinsic record, and any extrinsic evidence. *See Uship Intellectual Props., LLC v. U.S.*, 714 F.3d 1311, 1315 (Fed. Cir. 2013).

Fundamentally, when construing claims in light of the specification, we do so "with a view to ascertaining the invention." *United States v. Adams*, 383 U.S. 39, 49 (1966). Even when applying the broadest reasonable interpretation standard, which is broader than the standard applicable here, we have held that "[t]he correct inquiry . . . is not whether the specification proscribes or precludes some broad reading of the claim term adopted by the examiner." *In re Smith Int'l, Inc.*, 871 F.3d 1375, 1382–83 (Fed. Cir. 2017). Rather, a correct construction is one "that corresponds with . . . how the inventor describes his invention in the specification, i.e., an interpretation that is consistent with the specification." *Id.* at 1383 (citation and internal quotation marks omitted); *see also PPC Broadband, Inc. v. Corning Optical Commc'ns RF, LLC*, 815 F.3d 747, 752 (Fed. Cir. 2016).

II

Because the digital clock signals described in the '507 patent are periodic, *i.e.* they repeat at a regular interval, the variance or "phase difference" between two signals, A

and B, can in theory always be measured in one of two ways: (1) from a certain point on signal A to the next corresponding point on signal B (i.e., as the lag of signal B behind signal A), or (2) from a point on signal B to the next corresponding point on signal A (i.e. as the lead of signal B ahead of signal A). The question of whether a reference is referring to either or both of these measurements as the "phase difference" will depend on the context.

This is not unlike the ambiguity presented when we talk about the "time difference" between two analog clocks: The time difference between Clock A, which reads 1 o'clock, and Clock B, which reads 8 o'clock, could be 7 hours or 5 hours, depending on whether we are looking at the lag or the lead of Clock A relative to Clock B. If one is instructed to determine the time difference between these two clocks, and to maintain the time difference within 6 hours, that person would first need to understand what "time difference" means in the full context of the instruction.

Here, the Board recognized in its initial Institution Decision that the phrase, "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°," was facially ambiguous in that it "does not specify whether the input clock signal must be ahead of the feedback clock signal or the feedback clock signal must be ahead of the input clock signal." J.A. 867. Consistent with its obligations under *Phillips*, the Board looked to the specification for guidance, and determined that the patent's written description of the limitation at issue indicated that "phase difference" referred to the lag of the feedback clock signal behind the input clock signal:

> the Specification of the '507 patent makes a distinction between feedback clock signals that are more than 180° *behind the input clock signal* and feedback clock signals that are less than 180° *behind the input clock signal*. ['507 patent, col. 3 ll. 8-15].

> Indeed, when the feedback clock signal is determined to be more than 180° *behind the input clock signal*, a step is applied to invert it, effectively shifting it by 180°. *Id. That is the disclosed implementation for the limitation at issue*, i.e., "maintaining the phase difference between the input clock signal and the feedback clock signal [within] approximately 180°."

J.A. 868-889 (emphasis added).

This unidirectional understanding of "phase difference" is consistent with the usage of the term throughout the claims. Claim 10 recites the following steps:

> *determining a phase difference* between an input clock signal and a feedback clock signal;
>
> *maintaining the phase difference* between the input clock signal and the feedback clock signal [within] approximately 180°, including adjusting the input clock signal with a loop comprising a phase detector, shift register, and delay line *when the determined phase difference* is less than approximately 180°; and
>
> delaying the input clock signal to *compensate for the phase difference*, wherein a number of delay cells utilized is reduced by approximately one-half.

'507 patent, col. 4 ll. 49–59 (emphasis added). The "phase difference" determined in the first step is the antecedent for the "phase difference" in the subsequent steps, and thus the claim term should be construed to have a consistent meaning, including with respect to directionality, in each step. *See Phonometrics, Inc. v. Northern Telecom Inc.*, 133 F.3d 1459, 1465 (Fed. Cir. 1998) ("A word or phrase used consistently throughout a claim should be interpreted consistently."). The steps of determining a phase difference, maintaining a phase difference within a given range, and adjusting the input signal based on the determined

difference all indicate that the "phase difference" recited in the claim is meant to be a single measurable value: the term should not be construed to encompass two different "phase differences." Moreover, the phrase "delaying the input clock signal to *compensate* for the phase difference" indicates that the phase difference refers to the lag of the feedback clock behind the input clock. As a matter of common usage, if I say that I am delaying Clock A to compensate for the time difference between Clock A and Clock B, I am implying that Clock B is behind Clock A.

Additional intrinsic evidence supports the construction of "phase difference" as unidirectional. In particular, the '507 patent teaches that maintaining the phase difference within 180° by inverting (or shifting by 180°) the input signal when the phase difference is greater than 180° reduces the length of the delay line needed to compensate for the phase difference. '507 patent, col. 3 ll. 7-18; col. 4 ll. 35-42. This only makes sense if the "phase difference" at each step is consistently measured in one direction.

III

Neither the Board nor the Majority refute or even engage with this analysis in arriving at the plain meaning of the claim language. Indeed, when the Board revised its construction of "maintaining a phase difference . . . [within] approximately 180°" in its Final Written Decision, the Board pointed to nothing in the '507 patent that indicated a bi-directional usage of "phase difference." Rather, the decision reframed the facial ambiguity identified in its institution decision as linguistic clarity: "The words of the claim are *clear in not specifying* which signal leads or lags." J.A. 17 (emphasis added). The Board then proceeded to explain why the intrinsic evidence supporting a directional limitation does not amount to "express disavowal" justifying "rewriting" of the claims. *Id.*

The majority relies on essentially the same reasoning. Citing only to the text of the "maintaining" limitation, and

without any further discussion, the opinion concludes in a single sentence that neither claim 8 nor claim 10 "states or implies that the phase difference between the two signals is calculated by how much the feedback signal 'follows' or lags behind the input signal." Slip op. 13. The opinion then proceeds to search the intrinsic evidence for lexicography or disavowal, and ultimately finds none. But if the skilled artisan would understand the plain and ordinary meaning of "phase difference" in the context of the patent to be unidirectional, then the patentee need not include additional verbiage to narrow the scope of its claims from some other broader meaning. Ultimately, nowhere does the majority conduct the principal analysis of determining the plain and ordinary meaning of the claim language, including the words "phase difference," in the context of the patent. This is error.

Nothing in the majority's remaining analysis mitigates this deficiency. The mere fact that another independent claim, claim 13, recites "determining whether a feedback clock signal in the DLL *follows* within a 180° phase difference *behind* an input clock signal" does not contradict the consistent directionality of the "phase difference" described throughout the patent. Slip op. at 15 (quoting '507 patent, col. 4 l. 66–col. 5 l. 10). We have previously acknowledged that a patentee's choice to use different, though similar, words for corresponding limitations in different claims "does not mandate different interpretations of the two limitations . . . ." *Kraft Foods, Inc. v. Int'l Trading Co.*, 203 F.3d 1362, 1368 (Fed. Cir. 2000) (internal quotations and citation omitted). Here, in particular, the use of the words "follows" and "behinds" in one claim and not others does not implicate the doctrine of claim differentiation because the claims contain different steps that confer different claim scope separate and apart from the language at issue. *Cf., id*. at 1366 (noting that the doctrine of claim differentiation is based on the presumption that two claims in the same patent have different claim scope).

Likewise, a bi-directional construction of "phase difference" cannot rest on the conclusion that the construction does not *always* render the "maintaining" limitation superfluous and meaningless. Slip Op. 17-19. More relevant here is the canon that in cases of genuine ambiguity, claims are to be construed in favor of preserving validity. *Ruckus*, 824 F.3d at 1004 (citing *Phillips*, 415 F.3d at 1327). Here, except in those circumstances where the "maintaining" limitation is functionally meaningless, the majority's bi-directional reading of "phase difference" renders the claims at issue indefinite because it encompasses two different ways of determining the phase difference with no guidance on which to apply for any given claim, precluding a skilled artisan from discerning with "reasonable certainty" whether the "maintaining" limitation is satisfied. *See Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335, 1345 (Fed. Cir. 2015).

Ultimately, there is sometimes a fine line between "using the specification to interpret the meaning of a claim and importing limitations from the specification into the claim." *Phillips*, 415 F.3d at 1323; *Intervet Am., Inc. v. Kee–Vet Labs., Inc.*, 887 F.2d 1050, 1053 (Fed. Cir. 1989) (cautioning against confusing "interpreting what is meant by a word in a claim" with "adding an extraneous limitation appearing in the specification"). Here, the Board avoided its obligation to engage in the former task by mistaking it for the latter. The majority joins the Board in misjudging the line.

For these reasons, I would reverse the Board's claim construction. Because Samsung has made no argument that the invalidation of the claims at issue could be affirmed under ProMOS's construction, I would reverse the invalidation of those claims as well.