NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

LONE STAR SILICON INNOVATIONS LLC,
Appellant

v.

ANDREI IANCU, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2019-1556

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2017-01562.

Decided: May 14, 2020

TIMOTHY P. MALONEY, Fitch, Even, Tabin & Flannery, Chicago, IL, for appellant. Also represented by NICHOLAS T. PETERS, DAVID ALLEN GOSSE.

FARHEENA YASMEEN RASHEED, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA, for intervenor. Also represented by THOMAS W.

KRAUSE, AMY J. NELSON, MOLLY R. SILFEN, MEREDITH HOPE SCHOENFELD.

Before CHEN, HUGHES, and STOLL, *Circuit Judges*.

CHEN, *Circuit Judge*.

Lone Star Silicon Innovations LLC (Lone Star) appeals from the Final Written Decision by the Patent Trial and Appeal Board (Board) in *inter partes* review (IPR) No. IPR2017-01562. The Board held that all challenged claims of U.S. Patent No. 6,097,061 (the '061 patent), claims 1, 3–6, 11, and 13–16, are unpatentable. Lone Star's appeal centers on the Board's claim construction of the phrase "a channel region formed in the semiconductor substrate" in independent claims 1 and 11 and obviousness conclusion for dependent claims 6 and 16.

Because the Board correctly applied the established ordinary meaning in the art for the "channel region" limitation and we see no error in the Board's conclusion of obviousness for dependent claims 6 and 16, we *affirm*.

BACKGROUND

The '061 patent, entitled "Trenched Gate Metal Oxide Semiconductor Device and Method," is directed to a Metal Oxide Semiconductor (MOS) transistor having a trenched gate.[1] '061 patent col. 1 ll. 46–57. Conventional MOS transistors include a semiconductor substrate having a source region, drain region, and a channel region between the source and drain regions, with a gate dielectric layer and a

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[1] Lone Star argues that the '061 patent is also directed to methods of manufacture, but all the claims are for a semiconductor device. A subsequent divisional patent sets forth manufacturing method claims. *See* U.S. Patent No. 6,667,227.

gate electrode layer disposed on the top surface of the semiconductor substrate directly above the channel region. *Id.* at col. 1 ll. 28–34. According to the patent, having the gate formed on top of the substrate limits "the degree to which active devices can be made smaller in order to improve packing density and performance." *Id.* at col. 1 ll. 41–43.

The specification describes its solution to this problem in the "Summary of the Invention" section: "In accordance with the present invention, a semiconductor device is fabricated to include a trenched polysilicon gate which is formed in a trench of a semiconductor substrate." *Id.* at col. 1 ll. 46–48. The patent goes on to say that positioning the gate within a trench in the substrate provides benefits over conventional gate structures, including "better process control and improved manufacturability." *Id.* at col. 1 ll. 49–51. In addition, "[t]he trenched polysilicon gate structure of the present invention" improves the device packing density and scalability. *Id.* at col. 1 ll. 51–55. The patent then describes a number of different embodiments showing how the trenched gate is incorporated into an otherwise standard MOS transistor, each embodiment disclosing a source region, drain region, and channel region in combination with a trenched gate.

Claim 1 is representative and recites:

> 1. A semiconductor transistor comprising:
>
> a semiconductor substrate of a first conductivity type;
>
> a source region of a second conductivity type in the semiconductor substrate;
>
> a drain region of the second conductivity type spaced from the source region in the semiconductor substrate;
>
> a trench having substantially upright vertical surfaces and a bottom surface formed in the

> semiconductor substrate intermediate the source and drain regions;
>
> *a channel region formed in the semiconductor substrate*, the channel region forming a contiguous region beneath the bottom surface of the trench and immediately contiguous to the source and drain regions;
>
> a trench-to-gate insulating layer formed on the substantially upright vertical surfaces and the bottom surface inside the trench, the trench-to-gate insulating layer forming a contiguous layer inside the trench; and
>
> a trenched gate electrode having a top surface and formed on the trench-to-gate insulating layer inside the trench.

'061 patent claim 1 (emphasis added).

On June 9, 2017, Micron Technology, Inc. (Micron) filed an IPR petition against the '061 patent challenging claims 1, 3–6, 11, and 13–16. The Board instituted the IPR, and issued its Final Written Decision, finding all challenged claims unpatentable. *Micron Tech. Inc. v. Lone Star Silicon Innovations LLC*, IPR2017-01562, at 40 (P.T.A.B. Dec. 13, 2018). Specifically, the Board found that claims 1, 3–5, 11, and 13–15 would have been obvious over U.S. Patent No. 5,408,116 (Tanaka), claims 6 and 16 would have been obvious over Tanaka and U.S. Patent No. 5,283,449 (Ooka), and claims 1, 3, 4, 11, 13, and 14 would have been obvious over U.S. Patent No. 5,300,447 (Anderson). It is undisputed that both Tanaka and Anderson are directed to MOS transistors having a gate formed in a trench within the semiconductor substrate. Appellant's Br. at 13, 20.

In a thorough, extensive analysis, the Board construed the phrase "a channel region formed in the semiconductor substrate" recited in independent claims 1 and 11.

Applying the *Phillips v. AWH Corp.* standard,[2] the Board rejected Lone Star's proposed claim construction of "a channel region defined by the presence of dopants that are separate or additional relative to the semiconductor substrate of a first conductivity type." *Micron*, IPR2017-01562, at 8 (citing 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc)). The Board found that, while the claim term encompassed a channel region implanted with an additional or separate dopant, neither the claim language itself nor the specification limited the claimed "channel region" to require that attribute. Rather, the Board concluded that it should apply the well-established ordinary meaning of this claimed phrase in the MOS transistor art: "the region circumscribed by the gate, gate oxide, source, and drain in a transistor; that is, the place in the transistor where a channel forms during normal operation or use, regardless of whether the channel is doped differently than the substrate." *Id.* at 9, 23–24. In other words, the "textbook way" of forming a channel region in the substrate for a MOS transistor was through the formation of the surrounding source, drain, and gate structures. *Id.* at 9.

As to the specification, the Board recognized that it described a number of illustrative examples in which the channel region is implanted with a dopant. But because those references to an implanted channel region consistently were in the context of describing "one embodiment" or a "preferred embodiment" of the invention, the Board found these references to be only "exemplary in nature" and declined to read the limitation of implanting a dopant into the claimed "channel region." *Id.* at 21–22.

Instead, the Board agreed with Micron that a skilled artisan in the relevant art would understand that "a

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[2] The Board applied the *Phillips* standard because the patent had expired. *Micron*, IPR2017-01562, at 8 (citing *In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012)).

channel region" can be formed in relation to the source, drain, and gate structures. The Board relied heavily on a college textbook discussing the typical structure of MOS transistors. ADEL S. SEDRA & KENNETH C. SMITH, MICROELECTRONIC CIRCUITS (3d ed. 1991) (Sedra). More particularly, the Board relied on Sedra's Figure 5.1 below showing a standard MOS transistor.

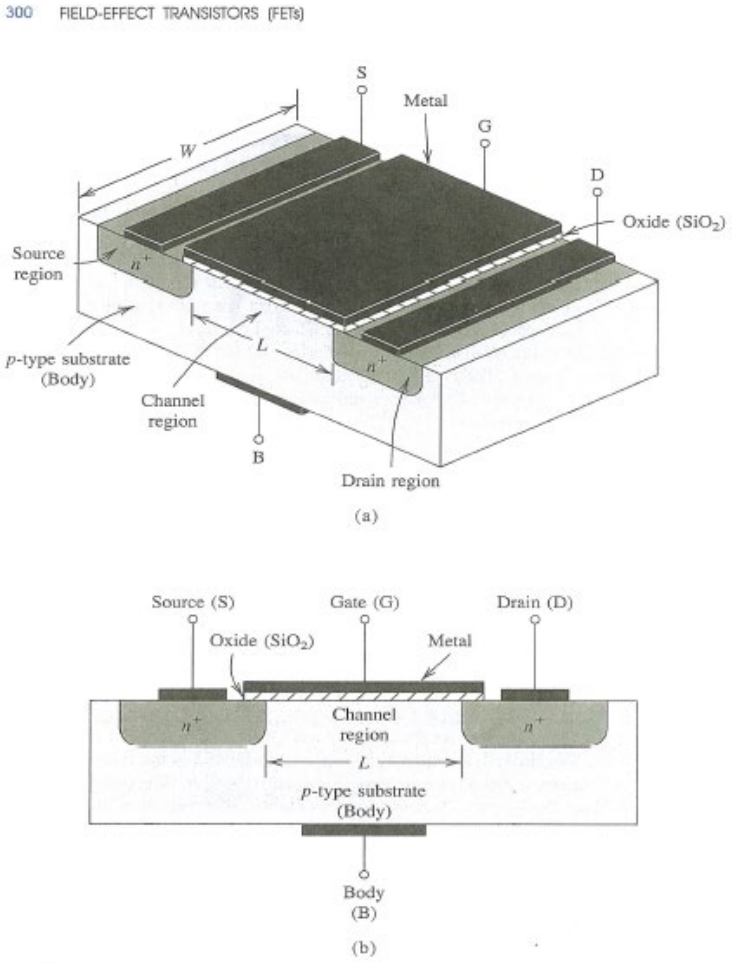

Fig. 5.1 Physical structure of enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically $L = 1$ to 10 μm, $W = 2$ to 500 μm, and the thickness of the oxide layer is of the order of 0.1 μm.

Id. at 300.

The Board stated, "Figure 5.1 includes perspective and cross sectional views of the physical structure of an *n*-type metal oxide semiconductor ('NMOS') transistor, and depicts a channel region in relation to the other transistor structures, including the gate, gate oxide, source, drain, and substrate body of the semiconductor device." *Micron*, IPR2017-01562, at 13; *see also id.* at 14 (discussing Sedra's equivalent disclosure for a p-type transistor). Sedra explains and illustrates that the "channel region" refers to the region of the substrate underneath the gate and bounded by the "source region" and "drain region," where "current will flow" once a voltage is applied to the gate. SEDRA, *supra* at 301. The Board also pointed to Anderson and *Principles of CMOS VLSI Design: A Systems Perspective*, by Neil H.E. Weste & Kamran Eshraghian (the Weste treatise), as further evidence showing that skilled artisans at the time of the invention understood that a MOS transistor channel does not require any separate doping, but instead can be defined by the formation of the surrounding source, drain, and gate. *Micron*, IPR2017-01562, at 15. Additionally, the Board noted that Lone Star's expert, Dr. Bottoms, conceded that textbooks provided the standard use of the term "channel region" as referring to the region between the source and drain where an induced current will be formed when a voltage is applied to the gate. *Id.* at 14 (citing J.A. 1713–14). Because the Board concluded that nothing in the claims or specification conveyed with sufficient clarity an intent to alter the established meaning in the art for "channel region formed in a semiconductor substrate," it construed the claimed phrase in keeping with its established meaning. Given that claim construction, the Board found all of the challenged claims unpatentable for the reasons raised by the petitioner.

Lone Star appealed. We have jurisdiction pursuant to 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

I. Claim Construction

Claim construction is as a question of law that may involve underlying fact inquiries. *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 326 (2015); *Wi-LAN USA, Inc. v. Apple Inc.*, 830 F.3d 1374, 1381 (Fed. Cir. 2016). This court reviews the Board's claim construction based solely on intrinsic evidence de novo, and reviews subsidiary fact findings as to extrinsic evidence for substantial evidence. *HTC Corp. v. Cellular Commc'ns Equip., LLC*, 877 F.3d 1361, 1367 (Fed. Cir. 2017).

When construing the claims of an expired patent, the Board applies a district court-type claim construction standard. *See In re Rambus*, 694 F.3d 42, 46 (Fed. Cir. 2012). Under that standard, claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of invention in light of the claim language, the specification, and prosecution history. *Phillips*, 415 F.3d at 1312–17. We have explained that "there is no magic formula" for conducting claim construction, and what matters is not necessarily the sequence of steps in consulting various sources; "what matters is for the court to attach the appropriate weight to be assigned to those sources in light of the statutes and policies that inform patent law." *Id.* at 1324 (citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). While "in general, certain types of evidence are more valuable than others," a judge who encounters a disputed claim term has the discretion to consider, as a starting point, dictionaries, treatises and textbooks to understand how one of skill might use that claim term, "as long as those sources are not used to contradict claim meaning that is unambiguous in light of the intrinsic evidence." *Id.* at 1324. For example, our court has on occasion first ascertained the meaning in the relevant technical field of a term recited in a claim before

considering how the patentee used that term in the context of the patent. *See, e.g.*, *Ancora Techs., Inc. v. Apple, Inc.*, 744 F.3d 732 (Fed. Cir. 2014); *Starhome GmbH v. AT&T Mobility LLC*, 743 F.3d 849 (Fed. Cir. 2014). "A claim term should be given its ordinary meaning in the pertinent context, unless the patentee has made clear its adoption of a different definition or otherwise disclaimed that meaning." *Ancora*, 744 F.3d at 734. The patent may provide such a clear intent either expressly or by implication. *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016).

Lone Star contends that the Board incorrectly construed "channel region formed in the semiconductor substrate" in accordance with the well-established ordinary meaning in the MOS transistor art, because, in Lone Star's view, the patent claims and specification clearly require the channel region to be implanted with its own dopant. While the claim language and specification are always the most important sources of evidence to any claim construction inquiry, we agree with the Board in this case that the intrinsic evidence lacks the needed clarity to import a dopant implantation requirement into the claimed channel region.

The Board correctly found that the record shows that a "channel region formed in the semiconductor substrate" had a well-understood meaning in the MOS transistor art at the time of the invention. The term generally refers to the region of the substrate located under the gate and bounded by the source and drain regions in a MOS transistor. As Sedra, a standard college textbook in the field, illustrates in Figure 5.1, a "channel region" is defined by the formation of the surrounding source region, drain region, and gate, without this area requiring any separate processing or alteration with any additional dopants, for example. SEDRA, *supra* at 299–301. Sedra describes that what its figure labels as the "channel region" in the substrate is where current will flow between the drain and

source when a voltage is applied to the gate during use. *Id.* at 301.

Moreover, the testimony of Dr. Bottoms, Lone Star's own expert, was consistent with the view of Dr. Fair, Micron's expert, when Dr. Bottoms explained that the industry understanding of "channel region" was the region in the substrate "that's bounded by the gate and the source and the drain . . . . so that space in the substrate but under the gate and between the source and the drain is often referred to as a channel region." J.A. 1713–14; *see also* J.A. 1226, 1228 ("The formation of [the drain and source regions and gate structures] in turn forms the 'channel region' because it is these structures that delineate where the induced channel will form."), 1230 ("It is this delineation [of the channel region with the source/drain, gate oxide, and gate], that gives meaning to the word 'formed' because it forms or shapes the channel region."). In addition, the Weste treatise and Anderson further reinforce the Board's finding that skilled artisans understood that a channel is formed in the substrate through the formation of the source, drain, and gate, without any requirement for separate doping. NEIL H.E. WESTE & KAMRAN ESHRAGHIAN, PRINCIPLES OF CMOS VLSI DESIGN: A SYSTEMS PERSPECTIVE 41–42 (2d ed. 1993) (describing the channel as the "region immediately under the gate" and "between the source and the drain"); Anderson, at Abstract (describing first "forming a gate," "and then forming source and drain regions," "thus forming the transistor channel."). Despite Lone Star's arguments to the contrary, substantial evidence supports the Board's finding that the disputed phrase had a well-established, ordinary meaning in the relevant art, a meaning that did not require separate doping.

Considering "channel region formed in the semiconductor substrate" in the context of the claims and specification, one of ordinary skill would have understood that the inventors did not depart from the established, ordinary meaning of the phrase. As the Board correctly observed, the

language of the claims "nowhere mentions a channel region defined by the presence of dopants." *Micron*, IPR2017-01562, at 9. The claim language of "formed in a semiconductor substrate" does not itself alter the meaning of "channel region" from the ordinary understanding of this phrase. As explained above, skilled artisans understood that a channel region can be "formed in the substrate" simply through the formation of the surrounding structures that define the contours of the channel region. This phrase thus does not, by itself, require an interpretation different from the ordinary meaning. Lone Star's reliance on other usages of "formed" in the claims, such as "a trenched gate electrode . . . formed on the trench-to-gate insulating layer," is unpersuasive for the same reason: it fails to account for the established industry understanding of how a channel region is "formed" through the creation of its surrounding transistor structures. The claim does not indicate that it is using the phrase "channel region formed in the semiconductor substrate" any differently from the established ordinary meaning.

We also disagree with Lone Star that the Board's construction renders superfluous the claim phrase reciting "the channel region forming a contiguous region beneath the bottom surface of the trench and immediately contiguous to the source and drain regions." As an initial matter, it is not clear why this additional phrase would be considered superfluous under the Board's construction but not Lone Star's: its preferred construction of "channel region formed in the semiconductor substrate" already requires a dopant to be implanted in the channel region. If that is correct, then, based on Lone Star's "superfluous" argument, there would be no work to do for the follow-on "forming" phrase. Moreover, Lone Star's argument as to the meaning of the follow-on "forming" phrase fails for the same reason as the "formed" phrase, explained above. In any event, we do not see the Board's construction as necessarily rendering the "forming" phrase superfluous, given

that it clarifies, in the context of the assertedly novel trenched gate, that the inventors have defined the "channel region" to have the customary attribute of being contiguous with the source and drain regions, despite the existence of a trench. At bottom, Lone Star's arguments are premised on the view that the specification altered the meaning of "channel region formed in the semiconductor substrate," but, as explained below, we do not believe that to be the case.

After a careful review, we agree with the Board that the specification does not show a clear intent, either expressly or implicitly, to redefine the "channel region" limitation to require an additional dopant. To be sure, the specification discloses examples of a trenched gate MOS transistor in which the substrate is implanted with a dopant to form a channel region. *See, e.g.*, '061 patent col. 5 ll. 36–38. But each of the instances in which the specification discusses an implanted channel region is in the context of describing "one embodiment" or a "preferred embodiment" of the invention. *Id.* at col. 1 ll. 58, 62–64, col. 2 ll. 7–11, col. 3 ll. 20–23, col. 4 ll. 54–55, col. 5 ll. 36–45. These examples are "not sufficient to redefine" the meaning of "channel region." *See Ancora*, 744 F.3d at 735 (quoting *IGT v. Bally Gaming Int'l, Inc.*, 659 F.3d 1109, 1118 (Fed. Cir. 2011)) (ruling that the specification's description for a "preferred embodiment," which was consistent with descriptions of other disclosed embodiments, was not limiting).

Using a term the same way in all disclosed embodiments is not by itself sufficient to redefine a term with an established ordinary meaning in the art. *See Aventis Pharma S.A. v. Hospira, Inc.*, 675 F.3d 1324, 1330 (Fed. Cir. 2012) ("[I]t is . . . not enough that the only embodiments, or all of the embodiments, contain a particular limitation to limit a claim term beyond its ordinary meaning." (internal quotations omitted)); *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (stating

that a party may "narrow a claim term's ordinary meaning, but he cannot do so simply by pointing to the preferred embodiment or other structures or steps disclosed in the specification or prosecution history"). The specification "must have sufficient clarity to put one reasonably skilled in the art on notice that the inventor intended to redefine the claim term." *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1370 (Fed. Cir. 2005); *see also Innova/Pure Water, Inc. v. Safari Water Filtration Sys.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) ("[E]ven where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope." (internal quotation omitted)). Lone Star's citations to the contrary do not teach otherwise and are not persuasive. *See Enzo Biochem Inc. v. Applera Corp.*, 780 F.3d 1149, 1156 (Fed. Cir. 2015) (finding that "direct detection" was not in the scope of the claim because the court's "analysis of the totality of the specification[] clearly indicates that the purpose of this invention was directed towards indirect detection, not direct detection"); *Regents of Univ. of Minn. v. AGA Med. Corp.*, 717 F.3d 929, 935–36 (Fed. Cir. 2013) (holding that "the claim language fully supports" the court's claim construction and that the construction was further supported by the specification describing the term as part of the "present invention" that was disclosed in every embodiment); *PODS, Inc. v. Porta Stor, Inc.*, 484 F.3d 1359, 1366–67 (Fed. Cir. 2007) (construing "carrier frame" based on claim differentiation and finding that consistent usage and statements distinguishing the prior art in the prosecution history supported that definition).

Lone Star's noted specification statements neither define "channel region" nor exclude any portion of the established ordinary meaning. More specifically, the specification at no time excludes the textbook understanding of a channel region from falling within "channel region." Moreover, the specification never characterizes its

references to the "channel region" as part of the patent's inventive contribution, or providing particular advantages or a novel distinction over prior art MOS transistors. *See SunRace Roots Enter. Co. v. SRAM Corp.*, 336 F.3d 1298, 1305 (Fed. Cir. 2003) ("[T]his is not a case in which a feature was described in the written description as critical but was never explicitly listed in the claim language, suggesting that the relevant structure in the claims should be narrowly construed as having that feature. Rather, in this case, the cam feature was explicitly included as an element in numerous claims, but not in the claim in suit."); *see also SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1343–44 (Fed. Cir. 2001) (finding that "the SciMed patents distinguish the prior art on the basis of the use of dual lumens and point out the advantages of the coaxial lumens used in the catheters that are the subjects of the SciMed patents" and that the specification included these dual lumens as part of "the present invention"); *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1371 (Fed. Cir. 2003) ("[T]he '907 specification indicates that the invention is indeed exclusively directed toward flooring products including play. Moreover, unlike the patent-at-issue in *Sunrace*, the '907 specification also distinguished the prior art on the basis of play."). In this case, the specification characterizes just one particular feature that "advantageously improves" "the present invention" over "conventional MOS circuits"—the trenched gate. Accordingly, we conclude that the Board properly weighed the various sources of evidence and correctly rejected Lone Star's proposed claim construction.

II. Dependent Claims 6 and 16

For claims 6 and 16, Lone Star also challenges the Board's finding that these dependent claims would have been obvious in view of Tanaka and Ooka. Lone Star contends that the Board did not give appropriate consideration to its arguments that the two references are incompatible. We find that the Board reasonably considered and weighed

Lone Star's arguments, and we agree with the Board's ultimate conclusion of obviousness.

The references themselves provide evidence supporting a finding that a skilled artisan would have been motivated to combine the tungsten silicide layer onto the Tanaka gate structure. As the Board found, Tanaka discusses that resistance increases in semiconductors can result in slower operating speed. Tanaka col. 1 ll. 10–20, col. 3 l. 68–col. 4 l. 2; Ooka col. 1 ll. 18–33; *see also Micron*, IPR2017-01562, at 34–35. Ooka specifically addressed this challenge by providing a tungsten silicide layer onto the gate to lower resistance. Ooka col. 1 ll. 34–44. Further, Ooka states that its teachings are for "semiconductor integrated circuit devices including MOSFETs." *Id.* at col. 1 ll. 18–25. Ooka also specifically stated that adding such a silicide layer was a recent trend in the art (i.e., was known at the time), and contemplated ways to fix certain complications created by these layers. *Id.* at col. 1 ll. 34–44, col. 1 l. 62–col. 2 l. 25. We agree with the Board that nothing in these teachings suggests that the two references would not be combined. Moreover, the Board relied on Micron's expert, Dr. Fair, who explained that conventional methods could have been used to properly include a layer of tungsten silicide on the top of Tanaka's gate electrode. *Micron*, IPR2017-01562, at 35 (citing J.A. 960).

The Board found Lone Star's incompatibility argument to be unpersuasive, amounting to "bare attorney argument." *Micron*, IPR2017-01562, at 36. In its Patent Owner Response, which was lengthy and made several different arguments, Lone Star briefly asserted that placing a silicide on top of Tanaka's gate electrode would introduce unwanted capacitance. J.A. 345. It also asserted that the silicide on the gate electrode "would likely short between the source and the drain." J.A. 346. While the Board did not expressly address these specific bases for incompatibility in its Final Written Decision, "the Board is 'not require[d] . . . to address every argument raised by a party or

explain every possible reason supporting its conclusion.'" *Yeda Research v. Mylan Pharm. Inc.*, 906 F.3d 1031, 1046 (Fed. Cir. 2018) (quoting *Synopsys, Inc. v. Mentor Graphics Corp.*, 814 F.3d 1309, 1322 (Fed. Cir. 2016), *overruled on other grounds by Aqua Prods., Inc. v. Matal*, 872 F.3d 1290, 1296 n.1 (Fed. Cir. 2017) (en banc)). Indeed, "[a]s we have said numerous times, failure to explicitly discuss every fleeting reference or minor argument does not alone establish that the Board did not consider it." *Id.* (citing *Novartis AG v. Torrent Pharm. Ltd.*, 853 F.3d 1316, 1328 (Fed. Cir. 2017)). Even assuming that the Board had failed to consider these arguments, they would not change the result here. Each of Lone Star's assertions included a pinpoint citation to the declaration of its expert, Dr. Bottoms. That declaration, however, fares no better than Lone Star's brief argument, because it provides little more than the same assertion without any meaningful additional support. Under these circumstances, we see no error in the Board rejecting Lone Star's skeletal arguments. *See TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1358 (Fed. Cir. 2019) ("Conclusory expert testimony does not qualify as substantial evidence."). Substantial evidence supports the Board's conclusion of obviousness for claims 6 and 16.

CONCLUSION

We have considered Lone Star's remaining arguments but find them unpersuasive. Consistent with the above, we affirm the Board's decision. We agree that the claim term "channel region formed in the semiconductor substrate" should be interpreted in accordance with its established ordinary meaning in the art at the time of the invention. We further find that there was substantial evidence supporting the Board's finding of obviousness for claims 6 and 16.

AFFIRMED

COSTS

No costs.