NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

NORTH STAR INNOVATIONS, INC.,
Appellant

v.

ANDREW HIRSHFELD, PERFORMING THE FUNCTIONS AND DUTIES OF THE UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2020-1874

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2019-00104.

Decided: November 4, 2021

EDWARD C. FLYNN, Eckert Seamans Cherin & Mellott, LLC, Pittsburgh, PA, argued for appellant. Also represented by PHILIP LEVY, NATHANIEL COEN WILKS.

WILLIAM LAMARCA, Office of the Solicitor, United

States Patent and Trademark Office, Alexandria, VA, argued for intervenor. Also represented by MAI-TRANG DUC DANG, THOMAS W. KRAUSE, FARHEENA YASMEEN RASHEED.

Before REYNA, SCHALL, and STOLL, *Circuit Judges*.

REYNA, *Circuit Judge*.

North Star Innovations, Inc. appeals the Patent Trial and Appeal Board's final written decision in an inter partes review determining that all of the claims of the challenged patent are unpatentable as anticipated and obvious. North Star specifically challenges the Board's constructions of the following claim terms: "a second phase signal that is opposite to the first phase signal," "second terminal coupled for receiving [a/the] boost signal," "inverting buffer," and "non-inverting buffer." Because the Board did not err in construing these terms, we affirm.[1]

BACKGROUND

I

North Star Innovations, Inc. owns U.S. Patent No. 6,127,875 ("'875 patent"). The '875 patent issued on October 3, 2000, and relates to "voltage boosting converters and, more particularly[,] to a double pumping voltage boosting circuit for providing an output voltage greater than a supplied input voltage and which is suited to be manufactured in integrated circuit form." '875 patent col. 1

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[1] North Star's opening brief included a challenge to the appointment of the Administrative Patent Judges involved in the underlying IPR. Appellant's Br. 67–70. Following the Supreme Court's decision in *United States v. Arthrex, Inc.*, 141 S. Ct. 1970 (2021), however, North Star withdrew its request to vacate and remand to the Board on this basis. ECF No. 49.

ll. 5–9. As shown in figure 3 below, the '875 patent teaches a double pumping voltage boost converter circuit that includes two sides—sides A and B—that "complement" each other during operation. *See id.* at col. 2 ll. 18–65. Put simply, sides A and B take turns supplying a boost signal. *See id.* at col. 2 ll. 38–65.

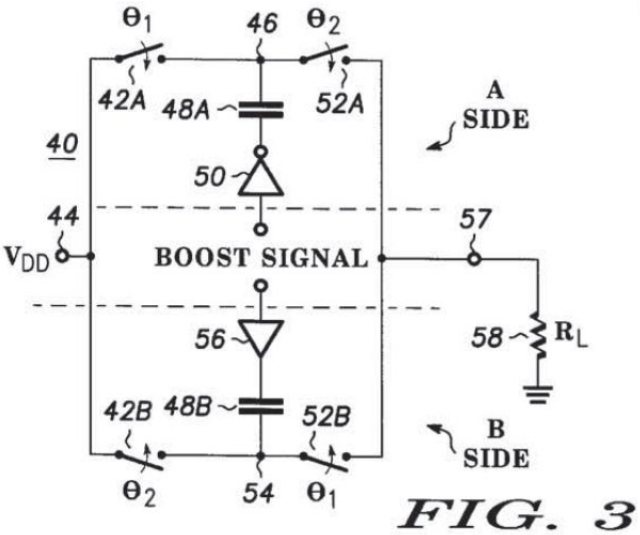

FIG. 3

Id. at fig. 3.

Figure 3 shows a preferred embodiment in which a voltage V_{DD} is supplied to the circuit. *Id.* at col. 2 ll. 15–28. During the first half cycle Θ_1, side B boosts the voltage. *See id.* at col. 2 ll. 18–65. Switches 42A and 52B are closed and switches 42B and 52A are opened. *Id.* at col. 2 ll. 38–40. Capacitor 48B resides "between terminal 54 and the non-inverting buffer driver 56." *Id.* at col. 2 ll. 31–33. Assuming capacitor 48B has already been charged to V_{DD}, the boost signal "is in a high level state" and raises the voltage across the capacitor to "nearly $2V_{DD}$," i.e., two times the supply voltage V_{DD}, to drive load 58. *Id.* at col. 2 ll. 40–46. As current flows from capacitor 48B into load 58, the charge across capacitor 48B begins to decrease. *Id.* at col. 2

ll. 46–48. But it does so "to a much less degree" than in prior art circuits represented by figure 1, *id.* at col. 2 ll. 46–48, and therefore the embodiment in figure 3 reduces voltage distortion, *see id.* at col. 1 ll. 57–61. While the voltage across capacitor 48B decreases, capacitor 48A is charged to voltage V_{DD}. *Id.* at col. 2 ll. 54–56.

Figure 2A shown below, together with figure 3, show that, at the end of the first half cycle Θ_1, clock signals C_1 and C_2 change phase so that side A boosts the voltage.

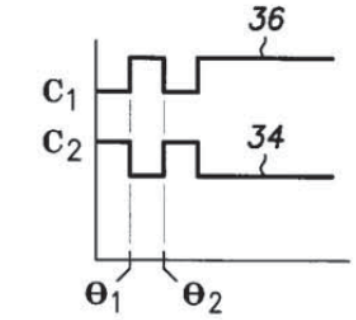

FIG. 2A

Id. at fig. 2A. The '875 patent describes C_1 and C_2 as a "pair of non-overlapping clock signals" that are "180 degrees out of phase with respect to one another." *Id.* at col. 1 ll. 32–34. In the second half cycle Θ_2, switches 42B and 52A are closed, whereas switches 42A and 52B are opened. *Id.* at col. 2 ll. 56–58. Capacitor 48A is positioned "between terminal 46 and inverting buffer driver 50." *Id.* at col. 2 ll. 28–30. The boost signal "changes states from a high level to a low level" and raises the voltage across capacitor 48A to nearly $2V_{DD}$, which then drives load 58. *Id.* at col. 2 ll. 56–63. Meanwhile, supply voltage VDD is applied across capacitor 48B. *Id.* at col. 2 ll. 59–63. According to the '875 patent, the preferred embodiment shown in figure 3 eliminates the need for an added load capacitance 28, as shown in figure 1 representing prior art, because "either

capacitive device 48A or capacitive device 48B is driving load 58 at all times." *Id.* at col. 3 ll. 3–7.

The '857 patent has three claims, all of which are at issue in this appeal. Claims 1 and 2, however, are representative of the issues in this appeal because they contain the disputed claim language, emphasized below:

> 1. A boost circuit having an input terminal and an output terminal, comprising:
>
> > a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;
> >
> > a second switch coupled between the input terminal and the output terminal and operated by *a second phase signal that is opposite to the first phase signal*;
> >
> > a first capacitor having a first terminal coupled to the output terminal and *a second terminal coupled for receiving a boost signal*; and
> >
> > a second capacitor having a first terminal coupled to the output terminal and *a second terminal coupled for receiving the boost signal*.
>
> 2. The boost circuit of claim 1, further including:
>
> > an *inverting buffer* having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and
> >
> > a *non-inverting buffer* having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor.

Id. at col. 5 l. 9–col. 6 l. 10 (emphasis added).

II

Kingston Technology Co. ("Kingston") filed a petition for inter partes review on October 19, 2018. J.A. 69–148. Kingston argued that claims 1–3 of the '875 patent were unpatentable as anticipated and/or obvious based on U.S. Patent No. 5,126,590 ("Chern"). J.A. 77. Chern is titled "High Efficiency Charge Pump" and relates to "charge pumps for biasing a semiconductor substrate, well, or the like, and more particularly, to a method and apparatus for efficiently, and therefore more quickly, biasing a substrate or well to a final desired voltage." Chern col. 1 ll. 5–9.

Chern's figure 2 shows an exemplary charge pump.

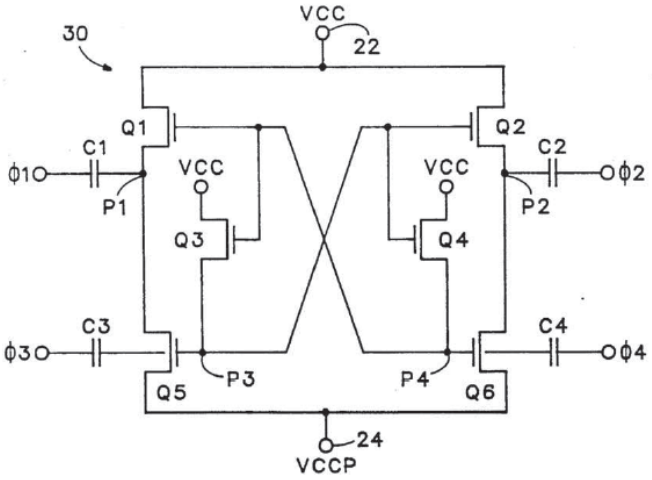

FIG. 2

Id. at fig. 2. Chern explains that terminal 22 receives a supply voltage VCC, *id.* at col. 3 ll. 20–22, and terminal 24 outputs a higher voltage VCCP, *id.* at col. 3 ll. 41–48. "[T]ransistors Q1–Q4 are coupled together," *id.* at col. 3 ll. 20–21, and transistors Q5 and Q6 "deliver current to the substrate or well," *id.* at col. 3 ll. 41–44. Capacitors C1–C4 each receive one of clock signals Φ1–Φ4 respectively, and each of the four capacitors is coupled to a combination of

transistors.[2] As shown in figures 6A and 6B, clock signals Φ1–Φ4 are driven by a ring oscillator 12 and a conditioning circuit 14 and are generated by a four-phase clock generator 42. *Id.* at col. 7 ll. 1–32. Chern explains that "clock generator 42 creates clock signals Φ1–Φ4 by providing delay paths" resulting in "an inverted and non-inverted half to create a total of four clock signals." *Id.* at col. 7 ll. 33–38.

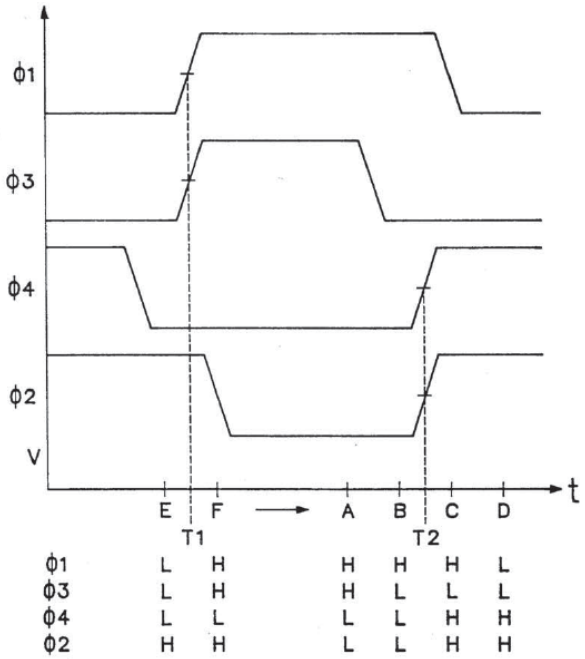

FIG. 3

[2] Capacitor C1 is coupled to transistors Q1 and Q5 at node P1; capacitor C2 is coupled to transistors Q2 and Q6 at node P2; capacitor C3 is coupled to transistors Q2, Q3, Q4, and Q5 at node P3; and capacitor C4 is coupled to transistors Q1, Q3, Q4, and Q6 at node P4. *Id.* at col. 3 ll. 24–41.

Id. at fig. 3.

Chern's figure 3 shows that each of the clock signals Φ1–Φ4 alternates between a "logic high state (H)" and a "logic low state (L)," such that the clock signals collectively undergo six intervals that Chern labels A through F. *See id.* at col. 3 ll. 61–68. As the interval sequence progresses, transistors Q5 and Q6 each take a turn delivering current to output terminal 24. *Id.* col. 5 ll. 9–12.[3] During the first half cycle, transistor Q5 delivers the current from capacitor C1, and meanwhile capacitor C2 charges. *Id.* at col. 5 ll. 16–20. During the second half cycle, transistor Q6 delivers the current from capacitor C2, and meanwhile capacitor C1 charges. *Id.* at col. 5 ll. 20–23. Notably, however, Chern's figure 3 shows brief periods at intervals B and E in which both clock signals Φ3 and Φ4 are at a logic low state. *See id.* at fig. 3.

III

The Board issued its final written decision on April 1, 2020, determining that challenged claims 1–3 of the '875 patent were anticipated by Chern and for that reason rendered the claims unpatentable under both §§ 102 and 103. *Kingston Tech. Co., Inc. v. N. Star Innovations, Inc.*, No. IPR2019-00104, 2020 WL 1581575, at *22 (P.T.A.B. Apr. 1, 2020) (citing *In re McDaniel*, 293 F.3d 1379, 1385 (Fed. Cir. 2002) ("It is well settled that anticipation is the epitome of

[3] At interval A, transistor Q5 delivers current to output terminal 24. *See* Chern at col. 4 l. 15. In the transition from A to B, transistor Q5 turns off. *Id.* As B transitions to C, transistor Q6 turns on and thus begins delivering current to terminal 24. *Id.* at col. 4 ll. 25–27. Transistor Q6 remains on until it turns off during the transition from D to E. *Id.* at col. 4 ll. 48–51. As E transitions to F, transistor Q5 turns on and remains on until the transition from A to B. *Id.* at col. 4 ll. 55–58.

obviousness." (quotation marks omitted))). The Board construed several claim phrases and then determined that Chern disclosed those phrases as construed.[4]

The Board first construed the phrase in claim 1, "a second phase signal that is opposite to the first phase signal," as not limited to signals that are "inverted" versions of each other. *Id.* at *5. The Board rejected North Star's narrow proposed construction requiring that the phase signals be "inverted" such that "the time during which the first phase signal is high is equal to the time during which the second phase signal is low and vice-versa." *Id.* at *3. The Board reasoned that the claim language did not expressly require North Star's proposed "inverted" limitation. *Id.* at *5. It further noted that the specification did not contain the word "opposite" and that it disclosed figure 3 as an exemplary depiction of opposing clock signals. *Id.* The Board rejected North Star's argument that extrinsic evidence proved that a person of ordinary skill in the art would have understood "opposite" clock signals necessarily as "inverted" signals. *Id.* at *3, *6. The Board explained that one such reference, U.S. Patent No. 5,644,534 ("Soejima"), which the examiner relied on during prosecution, disclosed clock signals that were "opposite" in phase yet not inverted. *Id.* at *6. For these reasons, the Board concluded that the record did not adequately support limiting the claim phrase to cover only clock signals that are inverted versions of each other. *Id.* at *5–6.

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[4] Because the '875 patent had expired on August 13, 2018, the Board applied the *Phillips* claim construction standard applied by district courts. *Id.* at *2 (citing *Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1376 (Fed. Cir. 2019); and then citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc)).

The Board then determined that Chern disclosed the phrase as construed. Kingston's petition identified Φ4, shown in Chern's figure 3, as corresponding to the first clock signal and Φ3 in the same figure as corresponding to the second clock signal. *Id.* at *13–14. Kingston also relied on a declaration by Dr. Jacob stating that Chern's Φ3 and Φ4 signals are "opposite" to each other because they "are the same signal, shifted 180 degrees (half a clock cycle) relative to one another," such that, "when clock Φ3 is high, clock Φ4 is low, and that when clock Φ3 is low, clock Φ4 is high." *Id.* at *14 (citation omitted). The Board rejected North Star's argument, predicated on its rejected claim construction, that Chern failed to disclose the "opposite" limitation because Chern's Φ3 and Φ4 clock signals are not inverted versions of each other. *Id.* at *14–15.

The Board also construed "boost signal" to mean "a signal that is input into a voltage boosting circuit for providing an output voltage greater than a supplied input voltage." *Id.* at *8. The Board rejected North Star's proposed construction limiting the term to require that "either a non-inverted or inverted version of [the boost] signal is received by the second terminal of a capacitor." *Id.* at *6–8. The Board reasoned that the '875 patent did not support limiting the claim scope as North Star proposed. *Id.*

The Board then determined that Chern disclosed the "boost signal" limitation. *Id.* at *16–17. According to Kingston, Chern's clock signals Φ1 and Φ2 constitute boost signals because they increase the voltage at node P1 and P2 respectively when the clock signals change from logic low state to logic high state. *Id.* at *17. These voltage increases in turn send current through transistors Q5 and Q6 respectively to drive the load through output terminal 24. *Id.* North Star's disagreement with Kingston's theory depended on its proposed claim construction requiring clock signals to be inverted versions of each other, which the Board rejected. *Id.* at *17–18.

The Board further construed "coupled for receiving" to mean "connected in order to receive." *Id.* at *9. The Board rejected North Star's argument that a person of ordinary skill in the art would understand the claim language to mean that the "terminal . . . is connected in a manner such that the signal received . . . is either always a non-inverted version of the boost signal or always an inverted version of the boost signal." *Id.* at *8. The Board again determined that the '875 patent did not support limiting the claim scope as proposed by North Star. *Id.* at *8–9.

The Board then determined that Chern disclosed the limitation as construed. *Id.* at *18. Kingston contended that Chern's capacitors C1 and C2 are coupled for receiving a boost signal (i.e., clock signals Φ1 and Φ2) because they are coupled by a circuitry path to clock generator 42, conditioning circuit 14 and ring oscillator 12, which collectively operated to create clock signals Φ1–Φ4. *See id.* The Board rejected North Star's argument, predicated on its proposed construction, that Chern was deficient because its clock signals underwent changes as they progressed through the circuitry leading to capacitors C1 and C2. *Id.* at *17–18. It was for that reason, North Star argued, that Chern's clock signals Φ1 and Φ2 are not "always" either an inverted or non-inverted version of the signal generated by the conditioning circuit 14, as its proposed claim construction required. *See id.* Because the Board rejected North Star's claim construction argument, the Board likewise rejected North Star's position that Chern failed to meet the "coupled for receiving" limitation. *Id.* at *18.

The Board also construed the phrase "inverting buffer" in claim 2 as not requiring either (1) a single input and single output, or (2) that the output is always an inverted version of the input. *Id.* at *9–10. North Star had proposed the following construction: "a circuit with a single input and a single output, where the output is always an inverted version of the input." *Id.* For support, North Star pointed to the fact that the '875 patent discloses an inverting buffer

in the form of a NOT gate and argued that "a NOT gate, also known as an inverter, is a single input, single output circuit whose output is always 1 if the input is 0, and whose output is always 0 if the input is 1." *Id.* at *9. The Board agreed with Kingston that, although figure 3 of the '875 patent discloses an embodiment where the inverting buffer has a single input and single output and the output is an inverted version of the input, nothing in the claim language or specification clearly supported limiting the claim scope to that embodiment. *Id.* at *9–10. For the same reason, the Board rejected North Star's narrow proposed construction of "non-inverting buffer" requiring "a circuit with a single input and a single output, where the output is always a non-inverted version of the input." *Id.* at *10.

The Board determined that Chern disclosed the "inverting buffer" and "non-inverting buffer" limitations. Kingston submitted annotated versions of Chern's figure 6B that identified the top half of clock generator 42 as an "inverting buffer" and the bottom half as a "non-inverting buffer." *Id.* at *19. Kingston's annotations, explained in Dr. Jacob's declaration, illustrated the behavior of all the logic gates in clock generator 42 when the input buffer signal is high or "1" and when it is low or "0." *Id.* Kingston also pointed to Chern's teaching that the clock generator 42 provided delay paths to create the four clock signals Φ1–Φ4. *Id.* The Board rejected North Star's arguments on the grounds that they were predicated on its proposed claim construction. *Id.* at *19–20.

North Star appealed the Board's final written decision that challenged claims 1–3 of the '875 patent are unpatentable under §§ 102 and 103 based on Chern. We have jurisdiction under 28 U.S.C. § 1295(a)(4).

DISCUSSION

I

We review the Board's "ultimate claim constructions de novo and its underlying factual determinations involving extrinsic evidence for substantial evidence." *In re Man Mach. Interface Techs. LLC*, 822 F.3d 1282, 1285 (Fed. Cir. 2016) (citations omitted). Obviousness under 35 U.S.C. § 103 is a question of law based on underlying facts. *In re Ethicon, Inc.*, 844 F.3d 1344, 1349 (Fed. Cir. 2017); *Mouttet*, 686 F.3d at 1330. We review the Board's legal conclusions of obviousness de novo and its factual findings underlying those determinations for substantial evidence. *In re Mouttet*, 686 F.3d 1322, 1330–31 (Fed. Cir. 2012). Anticipation under 35 U.S.C. § 102 is a question of fact, which we review for substantial evidence. *In re Gleave*, 560 F.3d 1331, 1334–35 (Fed. Cir. 2009). Substantial evidence is evidence that "a reasonable mind might accept as adequate to support a conclusion." *In re Gartside*, 203 F.3d 1305, 1312 (Fed. Cir. 2000) (quoting *Consol. Edison Co. v. NLRB*, 305 U.S. 197, 229–30 (1938)). Substantial evidence is "something less than the weight of the evidence but more than a mere scintilla of evidence." *In re Kotzab,* 217 F.3d 1365, 1369 (Fed. Cir. 2000). "[W]here two different, inconsistent conclusions may reasonably be drawn from the evidence in record, an agency's decision to favor one conclusion over the other is the epitome of a decision that must be sustained upon review for substantial evidence." *In re Jolley*, 308 F.3d 1317, 1329 (Fed. Cir. 2002) (citing *Grupo Indus. Camesa v. United States,* 85 F.3d 1577, 1582 (Fed. Cir. 1996)).

II

A

North Star argues that the Board erroneously construed the phrase, "a second phase signal that is opposite to the first phase signal," by declining to limit the phrase

to require that the two signals are "inverted versions of each other, such that the time during which the first phase signal is high is equal to the time during which the second phase signal is low and vice-versa." Appellant's Br. 18. We disagree and affirm the Board's construction.

The person of ordinary skill in the art is deemed to read a claim in the context of all the patent's claims, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314–17 (Fed. Cir. 2005). It is also permissible for courts, and the Board here, to rely on extrinsic evidence, such as dictionaries, treatises, and testimony of experts and inventors, with the understanding that such evidence "can shed useful light on the relevant art" but is generally "less significant than the intrinsic record." *Id.* at 1317. We have further recognized a fine line between "using the specification to interpret the meaning of a claim and importing limitations from the specification into the claim," and we have "repeatedly warned against" the latter. *Id.* at 1323; *see also SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) ("[A] particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment."); *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1302–03 (Fed. Cir. 2007) ("The mere fact that the specification's examples of translation may involve a change in protocol from a higher to a lower level protocol does not establish that such a limitation should be imported into the claims."). We have rejected the contention that, "if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment." *Phillips*, 415 F.3d at 1323. It is therefore improper to limit claims to a disclosed embodiment "absent a clear expression of intent to limit the claims' scope." *Info-Hold, Inc. v. Applied Media Techs. Corp.*, 783 F.3d 1262, 1266 (Fed. Cir. 2015).

North Star argues that the plain meaning of "opposite" is "inverted," and therefore the Board's interpretation

encompassing non-overlapping signals that are 180 degrees out of phase with each other—yet are nevertheless not inverted versions of each other—contradicts the term's plain meaning. Appellant's Br. 18–19. North Star relies on the opinion of its expert, Dr. Khatri, regarding how a person of ordinary skill in the art would have understood the plain language of the claim limitation at the time of invention. *Id.* at 20 (citing J.A. 1726 ¶ 102). However, we read the cited portions of Dr. Khatri's opinion as the type of conclusory testimony our court has described as "not useful." *Phillips*, 415 F.3d at 1318. Dr. Khatri cites no support for his opinion on this point. *See* J.A. 1726. North Star also attempts to support its position by pointing to the assertion in Kingston's petition and Dr. Jacob's supporting declaration that Chern's clock signals Φ3 and Φ4 are "opposite" to each other because when "clock [Φ]3 is high, clock [Φ]4 is low, and that when clock [Φ]3 is low, clock [Φ]4 is high." *Id.* at 20 (citing J.A. 115, 615 ¶ 152). But we are not persuaded that this assertion amounts to an admission that "opposite" signals include only inverted signals.

North Star next argues that the specification supports its interpretation of "opposite" as "inverted." North Star does not dispute that the '875 patent does not use the term "opposite." North Star nevertheless points to figure 2A as showing clock signals C1 and C2 that are inverted versions of each other, as well as the patent's description of figure 2A as showing "the clocking signals useful for explaining the operation of the present invention." *Id.* at 21–22 (citing '875 patent col. 2 ll. 1–2). North Star also relies on the specification's assertion that "either capacitive device 48A or capacitive device 48B is driving load 58 ***at all times***," and for that reason North Star argues that "all four switches are never open at the same time." *Id.* at 23 (quoting '875 patent col. 3 ll. 3–7). We are not persuaded that these disclosures clearly establish that the claim scope should be limited to only "inverted" signals. Figure 2A is described in the background section of the '875 patent in

the context of discussing not an embodiment but a "basic voltage boosting circuit" in the prior art. '875 patent col. 1 ll. 23–24. The background section also describes the clock signals C1 and C2 shown in figure 2A, not as "inverted" versions of each other, but rather as "non-overlapping" and "180 degrees out of phase with respect to one another." '875 patent col. 1 ll. 32–34. The detailed description section begins by discussing figure 3, which is described as "one embodiment of the present invention." *Id.* at col. 2 ll. 3–4. The '875 patent's teachings taken together lead to the conclusion that using "inverted" clock signals is an embodiment of the claimed inventions. This alone is not enough to limit the claim term "opposite" to only the narrow scope afforded by the distinct term "inverted." *Phillips*, 415 F.3d at 1323; *Superguide*, 358 F.3d at 875; *Verizon*, 503 F.3d at 1302–03.

North Star also argues that extrinsic evidence proves that a person of ordinary skill would understand the term "opposite" to mean only "inverted." However, certain references suggest that inverted signals are merely a subset of opposite signals. For example, Soejima teaches clock pulses having opposite phases and yet are not inverted. Soejima col. 5 ll. 38–40 & fig. 4B. U.S. Patent No. 5,701,096 ("Higashiho"), referenced by North Star on appeal, Appellant's Br. 28, teaches that its "second signal . . . *may be* an inverted signal of the clock signal." Higashiho col. 3 ll. 3–6. Further, Higashiho's claims expressly recite "inverted" clock signals, suggesting that the inventors of the '875 patent could have limited the claims to inverted signals if they had chosen to do so. *See, e.g.*, *id.* at col. 14 ll. 4–8, col. 15, ll. 28–32.

We conclude that the Board did not commit reversible error in rejecting North Star's argument that a person of ordinary skill in the art would have understood "opposite" as "inverted." Because North Star's arguments that Chern fails to disclose this limitation depend on its claim interpretation, we also affirm the Board's finding that Chern discloses this limitation.

B

North Star next argues that the Board erroneously construed "second terminal coupled for receiving [a/the] boost signal." Appellant's Br. 35. North Star contends that that language should be construed to mean that each of the first and second capacitors "is connected in a manner such that the signal received by that second terminal is either always a non-inverted version of the boost signal or always an inverted version of the boost signal." *Id.* at 36. We disagree and affirm the Board's construction that does not include the limitations North Star asks to be imported from the '875 patent's specification.

North Star contends that the plain language, "coupled for receiving," conveys "something more" than the second terminals of the capacitors being "coupled" to the boost signal or "coupled to a connection that is capable of receiving [the] boost signal." *Id.* at 38. Instead, North Star argues, the language "explicitly identifies which terminals, or connections, actually receive the boost signal." *Id.* Therefore, according to North Star, Chern's teachings that allegedly involve "intervening circuitry generat[ing] a ***new signal*** that is different from the boost signal" is not enough to satisfy the plain language. *Id.* at 39–40. For further support, North Star points out that the '875 patent "only describes one particular embodiment," and in that embodiment "the second terminals of the first and second capacitors actually receive either an inverted or non-inverted version of the boost signal." *Id.* at 40–41. We are not persuaded by North Star's narrow reading of the claim language that is tailored to certain details of the '875 patent's embodiment but not recited in the claims. Even where a patent only describes one embodiment, that is not enough to justify limiting broader claim language to unrecited details of that embodiment. *Phillips*, 415 F.3d at 1323. Because North Star's arguments that Chern fails to disclose this disputed claim language rests on its proposed construction, *see* Appellant's Br. 43–48, we also reject those arguments.

C

North Star finally contends that the Board erroneously construed "inverting buffer" and "non-inverting buffer" by rejecting its proposed constructions requiring "a single input and a single output" and that the output is "always" an inverted or non-inverted version, respectively, of the input. Appellant's Br. 48–49. We disagree and affirm the Board's constructions.

North Star contends that the Board improperly focused its construction on the term, "buffer," and failed to recognize that the complete terms, "inverting buffer" and "non-inverting buffer," refer to a "a particular kind of circuit, *i.e.*, one that has a single input and single output, where the output of the 'inverting buffer' is always inverted from its input, and the output of the 'non-inverting buffer' is always non-inverted from its input." Appellant's Br. 51. North Star does not persuasively explain or provide support for why the plain language conveys that meaning. North Star contends that the '875 patent's specification supports its construction by disclosing inverting buffer 50 as a NOT gate in figure 3. *Id.* at 53–54. North Star further points to a dictionary that defines a "NOT circuit" as a "binary circuit with a single output that is always the opposite of the single input" and that states that such a circuit is "[a]lso called [an] inverter circuit." *Id.* at 54 (quoting J.A. 1882–83). North Star also cites another extrinsic source showing an "inverter" as having "a single binary input variable and a single output binary variable." *Id.* (citing J.A. 1893–94). In support for its construction of "non-inverting buffer," North Star argues that the '875 patent uses the common electrical symbol of a "buffer gate" in its figures, arguing that "[i]t is well known that a buffer gate has the opposite functionality of a NOT gate." *Id.* at 54–55.

North Star thus points to examples, in the specification and certain extrinsic references, of inverting and non-inverting buffers that are consistent with its proposed

construction. We conclude that the Board's determination that the claim scope is not limited to those examples is not erroneous. The specification's use of certain electrical symbols in its figures does not necessarily mean that the claims are limited in the manner North Star argues. *Info-Hold*, 783 F.3d at 1266 ("[W]e have rejected the contention that it is proper to limit the claims to the single disclosed embodiment absent a clear expression of intent to limit the claims' scope."). Kingston's expert, Dr. Jacobs, opined that a buffer can have more than one input and need not always invert or not invert its input. *See* J.A. 1400–06 (discussing examples including tri-state buffers). We therefore reject North Star's arguments and affirm the Board's constructions of "inverting buffer" and "non-inverting buffer." And because North Star's arguments for patentability depend on its proposed constructions of those terms, we likewise reject those arguments.

CONCLUSION

We have considered North Star's remaining arguments but find them unpersuasive. For the reasons explained above, we conclude that North Star has not identified any reversible error in the Board's determination that Chern renders challenged claims 1–3 of the '875 patent unpatentable. We therefore affirm.

AFFIRMED

COSTS

No costs.