NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

INTEL CORPORATION,
Appellant

v.

PACT XPP SCHWEIZ AG,
Appellee

2022-1139

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2020-00539.

Decided: February 24, 2023

JOHN C. O'QUINN, Kirkland & Ellis LLP, Washington, DC, argued for appellant. Also represented by DIVA R. HOLLIS, NATHAN S. MAMMEN; ROBERT ALAN APPLEBY, JAMES E. MARINA, New York, NY.

SANFORD IAN WEISBURST, Quinn Emanuel Urquhart & Sullivan, LLP, New York, NY, argued for appellee. Also represented by NIMA HEFAZI, FREDERICK A. LORIG, Los Angeles, CA; MARK YEH-KAI TUNG, Redwood Shores, CA.

Before NEWMAN, PROST, and HUGHES, *Circuit Judges*.

PROST, *Circuit Judge*.

The Patent Trial and Appeal Board ("Board") determined that Intel, Inc. ("Intel") failed to prove certain challenged claims of U.S. Patent No. 9,552,047 ("the '047 patent") were unpatentable as obvious. *Intel Corp. v. PACT XPP Schweiz AG*, No. IPR2020-00539, Paper 35 (P.T.A.B. Sept. 8, 2021) ("*'539 Final Written Decision*"). We reverse.

BACKGROUND

Intel petitioned for inter partes review of several patents owned by PACT XPP Schweiz AG ("PACT"). Three resulting Board decisions are relevant to this appeal. First, in the '535 proceeding, the Board determined that Intel proved some, but not all, challenged claims of U.S. Patent No. 8,312,301 ("the '301 patent") were unpatentable as obvious. *Intel Corp. v. PACT XPP Schweiz AG*, No. IPR2020-00535, Paper 33, 2021 WL 3506785 (P.T.A.B. Aug. 9, 2021) ("*'535 Final Written Decision*"). Second, in the '541 proceeding, the Board determined that Intel proved all challenged claims of U.S. Patent No. 9,075,605 ("the '605 patent") were unpatentable as obvious. *Intel Corp. v. PACT XPP Schweiz AG*, No. IPR2020-00541, Paper 36, 2021 WL 8776166 (P.T.A.B. Aug. 31, 2021) ("*'541 Final Written Decision*"). And finally, in the '539 proceeding on appeal here, the Board determined that Intel proved some, but not all, challenged claims of the '047 patent were unpatentable as obvious. *'539 Final Written Decision*, at 87.

The '301, '605, and '047 patents all relate to optimizing power consumption in multiprocessor systems.[1] Power optimization is important for maximizing battery life and maintaining suitable temperatures for multiprocessor systems. There are a few ways to optimize power in a multiprocessor system, but the one at issue in this case focuses on adjusting "clock frequency." The clock frequency of a processor refers to the rate at which that processor can process data; the faster the frequency, the faster a processor can complete a task. *See id.* at 3.

Three claims of the '047 patent are representative for purposes of this appeal. We address each in turn.

I

Claim 2, in relevant part, claims a multiprocessor system

> wherein for at least some of the [processors], the clock frequency is adjustable at runtime *according to a state* of the multiprocessor system.

'047 patent claim 2 (emphasis added); *see* Appellee's Br. 6 n.1.

Intel relied on prior art reference Nicol[2] to teach this "according to a state" limitation. The Board concluded that Nicol failed to disclose this limitation because Nicol taught adjusting clock frequency only according to an "anticipated" state, and the Board construed the claim to require adjusting clock frequency according to an "existing" state. *'539 Final Written Decision*, at 15, 38.

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[1] "The '047 patent is a divisional of the '605 patent, and the '605 patent is a continuation of the '301 patent." Appellant's Br. 26.

[2] U.S. Patent No. 6,141,762 ("Nicol").

Without explanation as to why or how, the Board reached a contrary conclusion in the '535 proceeding when analyzing representative claim 12 of the '301 patent. Claim 12 of the '301 patent claimed a multiprocessor device

> wherein[] . . . the clock frequency of each [processor] is at least *determinable by a state* of the [multiprocessor] device

'301 patent claim 12 (emphasis added); *see* Appellee's Br. 6 n.1. In the '535 proceeding, the Board concluded that Nicol taught *that* "state" limitation even if "state" were construed to include only "existing" states. *'535 Final Written Decision*, 2021 WL 3506785, at *28.

II

Claim 7, in relevant part, claims a multiprocessor system that's

> adapted to . . . reduce the clock frequency *in accordance with a hysteresis characteristic[].*

'047 patent claim 7 (emphasis added).[3] In a generic sense, hysteresis is "[a]ny phenomenon in which there is a lag between the cause and the induced or observed effect." J.A. 2738; *see also* J.A. 2413 l. 20–2414 l. 11.

Intel also relied on Nicol to teach the "hysteresis characteristic" limitation of claim 7. But, according to the Board, Nicol did not disclose this limitation because the hysteresis in Nicol's system was the result of a

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[3] The original claim language reads "in accordance with a hysteresis characteristics." '047 patent claim 2. The parties agree that the final "s" in "characteristics" is a typo. *See* Appellant's Br. 57 n.9; Appellee's Br. 2. We accordingly refer to this limitation hereinafter as a singular "hysteresis characteristic."

"predetermined choice." *'539 Final Written Decision*, at 50 (cleaned up).

Yet in the '541 proceeding, the Board followed the opposite logic. There, Intel asserted that prior art Kling[4] taught the "hysteresis characteristic" limitation in representative claim 1 of the '605 patent. Claim 1 of the '605 patent claimed a method for operating a multiprocessor system in which

> the multiprocessor system . . . reduc[es] the clock frequency of . . . at least [a] part of the multiprocessor system *in accordance with . . . a hysteresis characteristic*.

'605 patent claim 1 (emphasis added). The Board found that Kling disclosed this limitation based on Kling's teaching of a system that implemented hysteresis "by comparing the same signal against two thresholds," *'541 Final Written Decision*, 2021 WL 8776166, at *16, where those two thresholds were predetermined by the user, *id.* at *21.

III

Claim 10, in relevant part, claims a multiprocessor system comprising

> a plurality of temperature sensors and a heterogeneous plurality of clocked [processors]; and wherein
>
> the multiprocessor having a plurality of regions, a temperature sensor being provided for each of said plurality of regions to measure the temperature of said specific region; and

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[4] U.S. Patent No. 6,367,023 ("Kling").

> the clock frequencies of said [processors] being dynamically adjustable in accordance with the sensed temperatures.

'047 patent claim 10; *see* Appellee's Br. 6 n.1. Intel argued, and PACT did not dispute, that a combination of Nicol and Bhatia[5] disclosed these limitations. But PACT did dispute that a person of ordinary skill would have been motivated to combine Nicol and Bhatia. The Board agreed with PACT. Although Intel had argued that a person of ordinary skill would have been motivated to use "Bhatia's approach of partitioning a system or chip into multiple thermal zones, each monitored by its own thermal sensor," with Nicol's system, *'539 Final Written Decision*, at 73 (cleaned up), the Board concluded that Intel's expert testimony that this approach would have been "beneficial" was "unsupported by record evidence," *id.* at 75 (citing J.A. 2772 ¶ 42).

This finding stands in direct contrast to the Board's finding that there was a motivation to combine Nicol and Bhatia in the '535 proceeding to render representative claim 3 of the '301 patent obvious. Claim 3 of the '301 patent claimed a method of operating a multiprocessor system by

> grouping . . . a plurality of subsets of [processors] . . .
>
> effecting a plurality of temperature measurements in different regions of the system; and
>
> based on the temperature measurement, . . . modifying clock rates of the plurality of subsets of [processors] . . . .

'301 patent claim 3; *see* Appellee's Br. 6 n.1. The Board found, in that proceeding, that Intel had demonstrated a

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[5] U.S. Patent No. 6,535,798 ("Bhatia").

person of ordinary skill would have thought it "beneficial" to combine Nicol and Bhatia to render this claim obvious because "a person of ordinary skill in the art would have understood that Bhatia's approach of partitioning a system or chip into multiple thermal zones, each monitored by its own thermal sensor, ... would improve the accuracy of Nicol's . . . system." *'535 Final Written Decision*, 2021 WL 3506785, at *18 (cleaned up).

Intel appeals the Board's '539 Final Written Decision with respect to claims 2–4, 7, 9–11, 13, and 27. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

Intel appeals the Board's determination that claims 2–4, 7, 9–11, 13, and 27 were not unpatentable as obvious. Intel asserts that the Board's conclusions are erroneous both on the merits and under the Administrative Procedure Act ("APA") as a result of the inconsistent conclusions between this proceeding and the '535 and '541 proceedings. Because we agree with Intel on the merits of each challenge, we need not address its APA arguments.

On the merits, Intel challenges the Board's claim construction of "state" for claims 2–4; claim construction of "hysteresis characteristic" for claims 7, 9, 13, and 27; and factual finding of no motivation to combine Nicol and Bhatia for claims 10 and 11.

Claim construction is a question of law reviewed de novo. *Data Engine Techs. LLC v. Google LLC*, 10 F.4th 1375, 1380 (Fed. Cir. 2021). Obviousness is ultimately a question of law reviewed de novo with subsidiary fact-findings, like motivation to combine, reviewed for substantial evidence. *PersonalWeb Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1381 (Fed. Cir. 2019). "Substantial evidence is such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." *Novartis AG v. Torrent Pharms. Ltd.*, 853 F.3d 1316, 1324 (Fed. Cir. 2017).

We agree with Intel on the merits of all claims on appeal and accordingly reverse.

I

Intel argues that the Board's determination that claims 2–4 were not unpatentable relies on an incorrect claim construction of "state." Appellant's Br. 44–50. We agree.

Claim 2 claims a multiprocessor system in which clock frequency for at least some processors "is adjustable at runtime *according to a state*." '047 patent claim 2 (emphasis added). The Board construed "according to a state" to require that "the clock frequency is adjusted as a result of, or in response to, an *existing* state of the multiprocessing system or its [processors]." *'539 Final Written Decision*, at 15 (emphasis added). In doing so, the Board explicitly credited PACT's argument that adjusting clock frequency "according to a state" excluded adjusting clock frequency according to an "anticipated" state. *See id.* at 11–13. The Board reasoned that anticipated-state clock frequency adjustments were excluded from the claim because the '047 specification describes changing clock frequency in response to only a variety of "preexisting" inputs, like the described "configuration state." *See id.* at 13–15.

On appeal, Intel argues that the Board's construction of "according to a state" is wrong because it excludes embodiments disclosed in the '047 patent. Appellant's Br. 44–45 (first citing *Oatey Co. v. IPS Corp.*, 514 F.3d 1271, 1276–77 (Fed. Cir. 2008); then citing *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014); and then citing *Golden Bridge Tech., Inc. v. Apple Inc.*, 758 F.3d 1362, 1365 (Fed. Cir. 2014)). PACT responds that the Board's construction is correct because the embodiments on which Intel relies aren't covered by the claim due to the claim's "at runtime" limitation. Appellee's Br. 28–30.

We start with the plain and ordinary meaning of the claim according to a person of ordinary skill. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "[C]lock frequency is adjustable at runtime according to a state of the multiprocessor system" does not limit "state" to existing states. That plain and ordinary meaning corresponds with the intrinsic evidence, which describes embodiments adjusting clock frequency according to an anticipated state. '047 patent col. 3 ll. 1–22; *id.* at col. 4 ll. 17–19; *id.* at col. 4 ll. 65–66.

PACT admits that the '047 patent describes embodiments that adjust clock frequency according to an anticipated state. However, PACT argues that "Intel [cannot] show that those [anticipated-state] embodiments concern claims 2–4" since claims 2–4 require clock frequency adjustment "at runtime." Appellee's Br. 29. PACT instead suggests that the anticipated-state embodiments concern other claims, like claim 1. Oral Arg. at 23:20–46, No. 22-1139, https://oralarguments.cafc.uscourts.gov/default.aspx?fl=22-1139_12072022.mp3. We are not persuaded by this argument. As an initial matter, the Board did not rely on the "at runtime" language to exclude the anticipated-state embodiments; it relied on the "according to" language. *See '539 Final Written Decision*, at 12. But even worse, PACT's argument makes no sense on the merits. Claim 1 also includes the "at runtime" limitation on which PACT relies. *See* '047 patent claim 1 ("[T]he clock frequency is adjustable at runtime . . . ."). And we discern no lexicography or disavowal excluding the anticipated-state embodiments from the scope of claims 2–4. *See Golden Bridge*, 758 F.3d at 1365.

Accordingly, we construe claims 2–4 to include adjusting clock frequency according to an anticipated state. The parties agree that, under such a construction, these claims are obvious, *see* Oral Arg. at 24:29–50, so we reverse the Board's contrary conclusion.

II

Intel argues that the Board's determination that claims 7, 9, 13, and 27 were not unpatentable relies on an incorrect claim construction of "hysteresis characteristic." Appellant's Br. 58–59. We agree.

Claim 7 claims a multiprocessor system that's "adapted to . . . reduce the clock frequency *in accordance with a hysteresis characteristic*." '047 patent claim 7 (emphasis added). The Board noted that the '047 patent "contains no helpful description" of what a hysteresis characteristic is. *'539 Final Written Decision*, at 46. So, without objection from PACT, the Board accepted Intel's "understanding" of "hysteresis" for the purposes of its analysis. *Id.* at 47. Intel, in part, described hysteresis as

> involv[ing] the nonlinear response of a circuit, in which the response to a particular set of input conditions depends both on the instantaneous values and the recent past of the input and output signal, with such behavior further characterized as the inability to retract exactly on the reverse swing of a particular set of input and output conditions.

Id.

Hysteresis is commonly used to avoid excessive switching. The parties agree that a modern thermostat is an example of a circuit that exhibits hysteresis, and we adopt PACT's description as illustrative:

> Suppose [a] thermostat's goal is to keep the room at *approximately* 70 degrees, and the thermostat is set to a window between 68 degrees and 72 degrees. Suppose further that the starting temperature before the thermostat is turned on is 66 degrees. Once turned on, the thermostat will trigger the heater to start, and the heater will stay on until the thermostat senses that the room's temperature is 72 degrees. At that point, the thermostat will tell

> the heater to turn off. The room's temperature will gradually decline during this "heater off" period until it reaches 68 degrees, at which point the thermostat will tell the heater to turn back on, and the cycle will repeat.

Appellee's Br. 39–40 (emphasis in original). Compare such a two-threshold system to one with a single threshold: suppose, still, that the thermostat's goal is to keep the room at approximately 70 degrees but that the thermostat turns the heater on and off as soon as the room temperature even slightly deviates from that single measure. The two-threshold thermostat avoids excessively switching the heater on and off using hysteresis, which results in energy savings.

On appeal, Intel argues that the Board implicitly and incorrectly construed "hysteresis characteristic" in determining that Nicol did not teach this limitation. Appellant's Br. 58–64. Intel asserts that the Board precluded "hysteresis characteristic" from covering systems that use programmed hysteresis, like the thermostat. *See id.* at 58–59. PACT responds that "the Board did not make a distinction between programmed hysteresis and naturally-occurring hysteresis." Appellee's Br. 40. According to PACT, the Board's construction "still involves a response by [a] programmed system" but requires that "that response is not entirely predetermined." *Id.* at 40–41 (cleaned up). To put that in terms of the thermostat, PACT says that a thermostat "adapted to . . . reduce the [room temperature] in accordance with a hysteresis characteristic" doesn't cover a thermostat that employs the two-threshold system if, say, the heater has a preset time following the room temperature reaching one of the thresholds before it turns on or off. *But see* J.A. 609 ("Lag is a form of hysteresis.").

We start with the plain and ordinary meaning of the claim according to a person of ordinary skill. *Phillips*, 415 F.3d at 1313. A "hysteresis characteristic," according

to the Board's understanding of "hysteresis," includes at least a "nonlinear response of a circuit" and an "inability to retrace exactly on the reverse swing of a particular set of input and output conditions." *'539 Final Written Decision*, at 47.[6] Neither of those characteristics preclude a predetermined response, and PACT points us to no other intrinsic or extrinsic evidence that otherwise indicates such a limitation is warranted.

Accordingly, we construe claims 7, 9, 13, and 27 to cover reducing clock frequency according to a hysteresis characteristic, even if that characteristic is the result of, in whole or in part, a predetermined choice. The parties agree that, under such a construction, these claims are obvious, *see* Oral Arg. at 37:17–32, so we reverse the Board's contrary conclusion.

III

Intel argues that the Board's determination that claims 10 and 11 were not unpatentable relies on a finding of no motivation to combine that lacks substantial evidence. Appellant's Br. 74–76. We agree.

There's no dispute that Nicol and Bhatia disclose all limitations of claims 10 and 11. The only dispute is whether an artisan of ordinary skill would have been motivated to combine those reference. *See* Appellee's Br. 48–49.

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[6] This means the claim covers a multiprocessor system "adapted to . . . reduce the clock frequency in accordance with," '047 patent claim 7, "a nonlinear response of [the] circuit" or an "inability to retrace . . . on the reverse swing" of that response, *'539 Final Written Decision*, at 47. The meaning of such a claim is unclear, but we need not resolve that question in the context of this appeal because the parties seem to agree that the dispute is whether a hysteresis characteristic may or may not be the result of a "deliberate choice." *See id.* at 50.

The Board found that such an artisan wouldn't have been motivated, explaining that Intel's argument that such a combination would have been "beneficial" lacked record evidence. *'539 Final Written Decision*, at 75.

The Board's rationale for finding a lack of motivation to combine is neither reasonable nor correct. The Board cited Intel's expert testimony in stating that Intel's motivation to combine argument was "unsupported by record evidence." *See id.* (citing J.A. 2772 ¶ 42). That expert testimony, in turn, cites to Bhatia, which explains that its "temperature sensor[s]" monitor and control corresponding "thermal zones" to maintain system temperature within a certain range. Bhatia col. 3 ll. 29–39; *see* J.A. 2772 ¶ 42 (citing Bhatia col. 3 ll. 29–39). Bhatia teaches that these temperature controls are useful because different processors can have different workloads; and a higher workload risks a high temperature; and a high processor temperature could cause circuit failure. Bhatia col. 1 ll. 5–59.

Intel's expert explained that it would be "beneficial" to implement a similar temperature control system with Nicol because "the different [processors in Nicol] can [also] have different workloads and thus different temperature profiles." J.A. 849 ¶ 249 (citing Nicol col. 5 ll. 42–44); *see* J.A. 2772 ¶ 41 (citing J.A. 849 ¶ 249). The cited passage of Nicol explains that different processors may be subject to different voltages; and a low voltage risks a low temperature; and a low processor temperature could also cause circuit failure. Nicol col. 5 ll. 42–44. And the relationship between workloads and voltage was well known in the art—the higher the workload, the higher the voltage needed to process that workload given a set period of time. *See id.* at col. 5 ll. 23–24, 42–44 (explaining that Nicol's system "react[s] to variations in the system['s] [work]load" by, in part, changing voltage supply).

We fail to see how this record evidence is lacking. The Board's citations directly explain how temperature

regulation is beneficial in monitoring and controlling multiprocessors since those processors could be subject to different voltages (like in Nicol) or different workloads (like in Bhatia). We thus reverse the Board's finding on motivation to combine and accordingly determine that claims 10 and 11 are obvious.

* * *

We reject the Board's claim construction of "state" and "hysteresis characteristic" and reverse its finding of a lack of motivation to combine Nicol and Bhatia.

CONCLUSION

We have considered PACT's remaining arguments and find them unpersuasive. For the foregoing reasons, we reverse the Board's judgment that claims 2–4, 7, 9–11, 13, and 27 are not obvious.

REVERSED