NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

MONTEREY RESEARCH, LLC,
Appellant

v.

STMICROELECTRONICS, INC.,
Appellee

2022-1411, 2022-1770

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2020-00990, IPR2020-01491, IPR2021-00704, IPR2021-00776.

Decided: October 26, 2023

KAYVAN B. NOROOZI, Noroozi PC, Los Angeles, CA, argued for appellant.

THERESA H. NGUYEN, Perkins Coie LLP, Seattle, WA, argued for appellee. Also represented by TYLER R. BOWEN, CHAD S. CAMPBELL, Phoenix, AZ; PHILIP ALCIDE MORIN, San Diego, CA.

Before DYK, TARANTO, and CHEN, *Circuit Judges*.

Opinion for the court filed by *Circuit Judge* CHEN.

Opinion dissenting in part and concurring in part filed by *Circuit Judge* DYK.

CHEN, *Circuit Judge*.

Monterey Research, LLC (Monterey) appeals the Patent Trial and Appeal Board's (Board) final written decisions determining all challenged claims of U.S. Patent No. 6,534,805 ('805 patent) unpatentable. *Advanced Micro Devices, Inc. v. Monterey Rsch., LLC*, No. IPR2020-00990, 2021 WL 6339618 (P.T.A.B. Nov. 23, 2021) (*990 Decision*); *Qualcomm Inc. v. Monterey Rsch., LLC*, No. IPR2020-01491, 2022 WL 682743 (P.T.A.B. Mar. 4, 2022) (*1491 Decision*). Because substantial evidence supports the Board's findings and we disagree with Monterey's claim construction argument, we *affirm* both decisions.

BACKGROUND

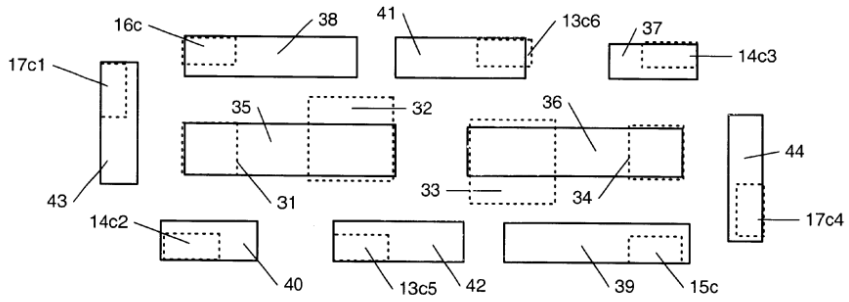
The '805 patent is directed to "an improved Static Random Access Memory (SRAM) cell design and method of manufacture." '805 patent col. 1 ll. 7–10. The parties' disputes concern, *inter alia*, claim 8, which reads:

> A memory cell comprising:
>
> > a plurality of substantially oblong active regions formed in a semiconductor substrate and arranged substantially in parallel with one another, and
> >
> > a plurality of substantially oblong local interconnects above said substrate that extend only partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to said active regions; and

> a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline.

Id. at claim 8.

The '805 patent describes a memory cell with multiple layers of material containing circuit components. *1491 Decision*, 2022 WL 682743, at *2. Local interconnects are short runs that connect features within a circuit, such as bitlines or a global wordline. '805 patent col. 11 ll. 18–21, col. 13 ll. 12–13, 31–32. Figure 3 of the '805 patent shows a top-down view of a single local interconnect layer as claimed in the final limitation of claim 8:



Id. at Fig. 3. Local interconnects 38 and 39 correspond to bitlines and are each associated with a single contact region (i.e., regions 16c and 15c). *Id.* at col. 13 ll. 12–14. Local interconnects 43 and 44 correspond to a global wordline are also each associated with a single contact region (i.e., regions 17c1 and 17c4). *Id.* at col. 13 ll. 31–32.

At the Board, the parties disputed the meaning of the last limitation in claim 8—"a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline." *1491 Decision*, 2022 WL 682743, at

*7.[1] While the parties agreed the claimed "single local interconnect layer" must contain local interconnects for both bitlines and a global wordline, they disagreed on whether the limitation is further limited. *Id.* Monterey argued that during prosecution the applicant limited the meaning of the disputed limitation to the embodiment in Figure 3, which, according to Monterey, requires a specific routing of signals laterally (i.e, horizontally) along the claimed local interconnects corresponding to the bitlines and global wordline. *Id.*; *see also id.* at *17 ("[T]he arguments are based on Patent Owner's proposed construction of 'a single local interconnect layer,' which requires routing all signals laterally along the interconnect layer."). Petitioner argued "neither the claim language nor the Specification support Patent Owner's proposed construction because neither uses the word 'routing'" and "Figure 3 does not 'illustrate any routing along the local interconnect layer' because the '805 patent does not 'illustrate any contacts atop the local interconnect layer, let alone specific positions that would demonstrate routing.'" *Id.* (quoting J.A. 10134).

The Board agreed with Petitioner and construed the term to mean "one conductive layer containing non-global interconnects, including interconnects for bitlines and a global wordline, that exclusively performs the function of connecting features within a circuit." *Id.* at *8. The Board concluded neither the specification nor prosecution history "limit[s] the single local interconnect layer limitation in the manner Patent Owner contends" because "although Figure 3 shows bitline signals *can* be routed horizontally . . . neither the Specification nor claims require such routing." *Id.* The Board further held the prosecution history does not disclaim any specific routing and instead disclaims the

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[1] Citations in this section are to the *1491 Decision*. The Board's construction and Monterey's proposed construction in the *990 Decision* were the same.

location of local interconnects in different layers of the cell. *Id.* According to the Board, the prosecution history shows Monterey distinguished the claimed memory cell over the prior art memory cell because the claimed memory cell limits the local interconnects corresponding to the bitlines and the global wordline to a single layer while the local interconnects in the prior art were found in multiple layers. *Id.* Thus, the Board agreed with Monterey that the disputed limitation restricts the local interconnects corresponding to the bitlines and the global wordline to one layer in the cell but declined to adopt Monterey's additional limitation of a specific lateral routing of signals along these local interconnects.

The Board also found the prior art reference Oh[2] disclosed "substantially oblong active regions." Monterey primarily argued Oh's figures fail to provide precise dimensions for the active regions shown. *Id.* at *13. The Board disagreed, finding "Petitioner [did] not rely on Figure 3 to demonstrate the precise dimensions of Oh's active regions. Instead, Petitioner relie[d] on Figure 3 to show the active regions have a 'substantially oblong' shape." *Id.* (citing J.A. 5024–26). The Board found Oh disclosed the general shapes of the illustrated active regions such that it taught the limitation. *Id.*

Monterey appeals. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

"We review claim construction de novo and review any subsidiary factual findings based on extrinsic evidence for substantial evidence." *Kyocera Senco Indus. Tools Inc. v. Int'l Trade Comm'n*, 22 F.4th 1369, 1378 (Fed. Cir. 2022). We generally give terms "their plain and ordinary meaning, which is the meaning one of ordinary skill in the art

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[2] U.S. Patent No. 6,417,549.

would ascribe to a term when read in the context of the claim, specification, and prosecution history." *Id.*

"The ultimate determination of obviousness is a question of law, but that determination is based on underlying factual findings," which we review for substantial evidence. *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379, 1381 (Fed. Cir. 2016). Substantial evidence is "such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." *Id.* at 1379–80.

I

Monterey argues its representations during prosecution limited the limitation "a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline" to a specific routing of signals laterally along the horizontal plane of the local interconnects as purportedly shown in Figure 3 of the '805 patent. Appellant's Br. 28 (arguing the Board "'disagreed' with Appellant's construction, 'which requires routing all signals laterally along the interconnect layer'"); *id.* at 38 (arguing Appellant's construction differentiates claim 8 over the prior art because the prior art's "bitlines are thus routed vertically through its layers, rather than laterally along a single local interconnect layer"). Monterey argues the Board erred by not including such limitation in its construction. But Monterey is wrong on two fronts—the applicant's representations during prosecution did not restrict the disputed limitation to the embodiment in Figure 3 of the '805 patent nor does Figure 3 limit the phrase as Monterey alleges.

Monterey cites a handful of pages in the prosecution history purportedly supporting its argument. Appellant's Br. 32–33 (citing J.A. 1262, 1812–13, and 1817–18). However, only one of these pages mentions Figure 3 and only does so by contrasting the single layer containing local interconnects in Figure 3 with the multiple layers containing local interconnects in the prior art. *See* J.A. 1262. The

other pages continue the same argument—the claimed single local interconnect layer distinguishes the invention from the prior art's local interconnects, which are located in multiple layers. *See* J.A. 1812–13, 1817–18. Thus, it appears applicant disclaimed local interconnects spread over multiple layers as opposed to locating all local interconnects in one layer. However, none of these prosecution statements refer to the relative size or length of the local interconnects portrayed in Figure 3. Nor do any of these statements suggest that the local interconnects provide connections between "laterally displaced" components, as Monterey alleges, thereby requiring signals to be routed along the length of the interconnects. Monterey simply never explains how the inclusion of the local interconnects on one layer requires the specific horizontal routing of signals along the local interconnect layer as it argues—a question also left unanswered by the dissent.

Separately, the embodiment shown in Figure 3 does not restrict the disputed limitation as Monterey argues. Figure 3 only shows a single contact region for each of the relevant local interconnects required by the disputed limitations—local interconnects 38, 39, 43, and 44. '805 patent Fig. 3 (showing contacts 16c, 15c, 17c1, and 17c4). Figure 3 does not show a second contact region associated with these local interconnects and thus is ambiguous as to whether their signals must be routed laterally along the interconnects. *See 1491 Decision*, 2022 WL 682743, at *8. We agree with the Board's construction.[3]

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[3] We acknowledge, as the dissent notes, the Board's statement that Figure 3 illustrates "routing bitline and wordline signals along an interconnect layer to connect laterally displaced bitlines and wordlines." *1491 Decision*, 2022 WL 682743, at *17. The Board, however, initially stated Figure 3 "shows bitline signals *can* be routed horizontally and a global wordline signal *can* be routed

II

Monterey also argues the Board improperly found that Oh disclosed "substantially oblong active regions." Monterey contends the Board could properly rely on Oh's figures only if the figures in Oh were drawn to scale, and Oh states the figures are not necessarily drawn to scale. We do not believe the Board misunderstood our case law and thus conclude the Board did not err in finding Oh's figures and specification disclose the general shapes of the claimed active regions. *See 990 Decision*, 2021 WL 6339618, at *9; *1491 Decision*, 2022 WL 682743, at *13.

CONCLUSION

We have considered Monterey's remaining arguments and find them unpersuasive. For the foregoing reasons, we affirm.

AFFIRMED

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vertically." *Id.* at *8. When read as a whole in light of the thrust of the opinion, the Board's decision is properly understood to mean Figure 3 shows the local interconnects *may* be routed horizontally or vertically, without requiring either. That is consistent with our reading of the figure.

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DYK, *Circuit Judge*, dissenting in part and concurring in part.

The majority affirms the Board's finding that the '805 patent is obvious over Oh. While I join part II of the majority opinion, I respectfully dissent from part I. Contrary to the majority opinion, I think the Board erred in holding that amendments made by the patentee during reexamination and the statements that accompany them did not narrow "single local interconnect layer" to require that all local interconnects be on a single layer that routes both bitline signals and a global wordline signal (the lateral construction).

I

Claim 8, as originally drafted, did not recite "single local interconnect layer" as a limitation and was not limited to the lateral construction. During reexamination, claim 8, without this limitation, was rejected as obvious over Osada, which all agree is a reference identical to Oh in relevant aspects. Monterey contends that Osada, like Oh, does not disclose a "single local interconnect layer" because it does not disclose that all local interconnects corresponding to the bitlines and a global wordline are in a single layer and, therefore, does not satisfy the lateral construction.

The patentee amended claim 8 to recite an additional limitation of "a single local interconnect layer comprising local interconnects corresponding to bitlines and a global wordline." J.A. 140, col. 1, ll. 33–35. In making this amendment, the patentee repeatedly explained the amendment was made to distinguish Osada. The prosecution history states:

> The Patent Owner then directed attention to the local interconnect layer of Fig. 3. . . . The Patent Owner observed that all the runs [(i.e., local interconnections)] for the bitlines, Vcc, Vss and the wordline are provided in the *single* layer of Fig. 3. The Patent Owner contrasted this aspect with Osada et al. . . . which shows *multiple* layers for its runs. The Patent Owner noted that this difference would lead to disadvantages of a thicker product and more processing steps in Osada than could be provided by the design in the '805 [p]atent.

J.A. 1262 (emphasis in original). The patentee cited Figure 3 and col. 13, ll. 12–14, 31–32 for support for its amendment. The patentee later "pointed out that the '805 [p]atent discloses local interconnects (LIs) in the *same* layer, as exemplified by LIs 38-39 for bitlines and LIs 43-

44 for a global wordline in Fig. 3 of the '805 [p]atent." J.A. 1812 (emphasis in original).

On its face, the amendments made during reexamination and the statements that accompany them appear to limit the claim to the lateral construction while referencing Figure 3. The Board agreed that without limiting the amended claim to this lateral construction the amended claim could not be distinguished over Osada (i.e., under the Board's construction the examiner erred in not maintaining the objection). Given the patentee's clearly articulated objective of overcoming the Osada rejection, I do not see how the amendments, and the accompanying statements, can be reasonably interpreted to not limit the scope of the claim to the lateral construction.

II

The majority urges that even if the prosecution history limited the claim to Figure 3, Figure 3 itself is not limited to the lateral construction. Maj. Op. at 6–7. But this is contrary to what the Board found. The Board found "the embodiment shown in Figure 3 of the '805 patent illustrates routing bitline and wordline signals along an interconnect layer to connect laterally displaced bitlines and wordlines." *1491 Decision*, 2022 WL 682743, at *17; *see also id.* at *8. The Board found it was the rest of the specification and the claim language that did not limit the scope of the claim to the embodiment of Figure 3, not that Figure 3 was not limited as such. Therefore, under the Board's findings, limiting the scope of the amended claim to the embodiment disclosed in Figure 3 would necessarily limit the scope to an embodiment that routes bitlines and a global wordline signals along an interconnect layer to connect laterally displaced bitlines and wordlines.

III

Under these circumstances, it seems to me that the prosecution history limited the claim to the lateral

construction, and thus the Board's contrary finding is incorrect. I respectfully dissent.