NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

MONTEREY RESEARCH, LLC,
Appellant

v.

KATHERINE K. VIDAL, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE,
Intervenor

2022-1577

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2020-01124.

Decided: December 12, 2023

DONALD LEE JACKSON, RIMON, PC, McLean, VA, argued for appellant.

BENJAMIN T. HICKMAN, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA, argued for intervenor. Also represented by PETER J. AYERS, FARHEENA YASMEEN RASHEED, PETER JOHN SAWERT.

Before TARANTO, CLEVENGER, and STOLL, *Circuit Judges*.

CLEVENGER, *Circuit Judge*.

Monterey Research, LLC ("Monterey") appeals an IPR decision[1] of the Patent Trial and Appeal Board ("Board") finding claims 1–19 of U.S. Patent No. 6,629,226 ("'226 patent") unpatentable. We *affirm*.

BACKGROUND

A. The '226 Patent

The '226 patent, titled "FIFO Read Interface Protocol," relates to a system of electrical circuits for storing data packets in a buffer memory and retrieving and moving said packets when a host system—such as a computer, disk drive, or other such logic system— cannot receive them due to insufficient memory or a busy network. The '226 patent is directed to "a method and/or architecture for implementing a multiqueue first-in-first-out (FIFO) memory read interface" to address synchronization issues and allow for the management of "variable-sized data packets." '226 patent, col. 1, ll. 16–29; *id.* col. 2, ll. 42–59. The "multiqueue FIFO memory" is claimed as a "multiqueue storage device" that stores data packets in multiple queues and is coupled to an interface ("read device") to read and orchestrate the retrieval of the data packets. *Id.* col. 9, ll. 50–67. Figures 3 and 4 of the '226 patent, replicated below, represent preferred embodiments, and demonstrate the relationship between the multiqueue storage device, the read device, and the handshaking signals used to implement the read protocol.

[1] *Advanced Micro Devices, Inc. v. Monterey Research, LLC*, No. IPR2020-01124, 2022 WL 213039 (P.T.A.B. Jan. 27, 2021) ("*Decision*").

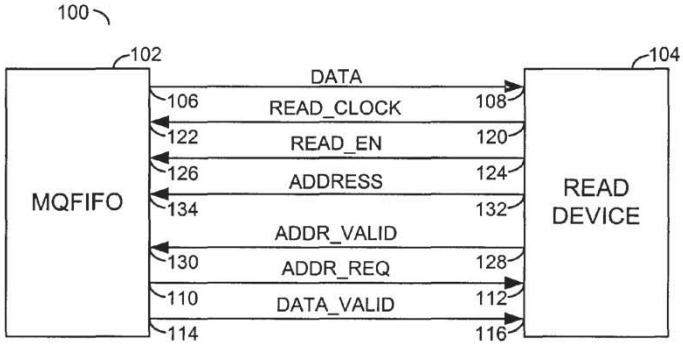

FIG. 3

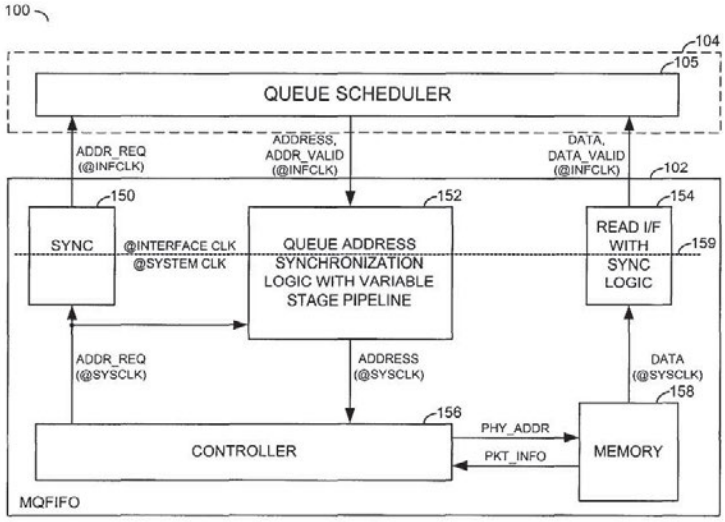

FIG. 4

'226 patent, Figs. 3 and 4.

As depicted in Figure 3 of the '226 patent, the claimed system is made up of a multiqueue storage device, depicted in the preferred embodiment as structure "MQFIFO" that interfaces with external read device through various signals. *Id.* col. 3, ll. 21–34. For example, MQFIFO sends an address request, labelled ADDR_REQ, to the read device, which returns a queue address, labelled "ADDRESS," and a validity signal, labelled "ADDR_VALID." J.A. 3 (citing

'226 patent, col. 3, ll. 35–46). The handshaking protocol that the system uses to transfer data is as follows: the ADD_REQ signal requests the next queue address, which causes the read device to return ADD_VALID, indicating that the queue address is valid. *Id.* col. 4, ll. 2–5. Then, MQFIFO asserts DATA_VALID and DATA in response. *Id.* col. 4, ll. 5–7.

As shown in Figure 4, the read device contains the queue scheduler, which manages the data queues in MQFIFO, and MQFIFO contains "synchronization circuit 150 [('SYNC 150')], address circuit 152, read interface circuit 154, controller circuit 156, and memory circuit 158." J.A. 5 (citing '226 patent, col. 4, ll. 51–65). The controller interacts with SYNC 150 and address circuit 152 by sending ADDR_REQ(@SYSCLK) to each component, after which SYNC 150 sends ADDREQ(@INFCLK) to the read device which returns ADDRESS(@INFCLK) and ADDR_VALID to address circuit 152. '226 patent, col. 5, ll. 3–9, 31–47. In response, address circuit 152 sends ADDRESS(@SYSCLK) to controller 156, which then sends PHY_ADDR to memory 158. *Id.* col. 5, ll. 10–14; *id.* col. 6, ll. 56–59, 64–67. The exchange of data signals and address validation "ensures that data is transferred when the queue address is valid." Appellant's Br. 4 (citing J.A. 52; J.A. 1232).

Claim 1 of the '226 patent is representative of challenged claims 1–19:

> 1. An interface coupled to a multiqueue storage device and configured to interface said multiqueue storage device with one or more handshaking signals, wherein said multiqueue storage device and said interface are configured to transfer variable size data packets and said multiqueue storage device is configured to generate an address request signal.

'226 patent, col. 9, ll. 51–58.

B. The Board's Claim Construction

The Board construed "'multiqueue storage device' as 'a storage device having data organized into multiple queues,' without any limitation on the logic or component that organizes or manages the queues—whether that logic or component is internal or external to the multiqueue storage device." *Decision*, 2022 WL 213039, at *5. Based on the intrinsic evidence, the Board determined that the '226 patent, while disclosing a "multiqueue storage device" that internally "includes the circuits that organize, manage, and control access to the data in the multiqueue storage device," did not limit "the multiqueue storage device to include internal management, organization, access control, and control of reading and writing of data into the multiqueue storage device." *Id.* The Board also considered extrinsic evidence to find that "a multiqueue storage device implicitly requires some component or logic that organizes or manages the queues" but that this does not require the device itself to contain the component that organizes the queues in the storage device. *Id.* The Board therefore concluded that it was not the case that "the multiqueue storage device itself must control access to reading and writing data to the queues in the multiqueue storage device." *Id.*

C. Anticipation by Joshi

Advanced Micro Devices, Inc.[2] challenged claims 1–19 of the '226 patent as anticipated by Joshi,[3] along with obviousness challenges based on combinations of other prior art references that are not at issue in this appeal. *Id.* at

---

[2] The parties have since settled and Advanced Micro Devices, Inc. has declined to participate in this appeal—thus, the Director of the United States Patent and Trademark Office has intervened to defend the Board's decision on appeal.

[3] U.S. Patent No. 4,949,301 ("Joshi").

*1–2. The Board decided that, since it found that claims 1–19 were anticipated by Joshi, it did not have to address the merits of the other grounds for invalidity. *Id.* at *16.

The Board found that, contrary to Monterey's arguments, Joshi disclosed a "multiqueue storage device" that is "configured to generate an address request signal." *Id.* at *9–16. The Board determined that Joshi's components DPC 43 and BM 38 met the limitation's requirement for a "multiqueue storage device" and that its components RBC 44 and FORMAC 34 comprised the "interface" that the "multiqueue storage device" is "coupled to." *Id.* at *8–10. The Board then concluded that, despite the intervening steps in Joshi's process, Joshi disclosed a "multiqueue storage device [] configured to generate an address request signal" because its signals DRDREQA and DRDREQS ultimately caused component RBC 44 to send the next packet address to BM 38. *Id.* at *12–14. Given the Board's findings regarding Joshi's teachings, it concluded that claims 1–19 of the '226 patent are anticipated by Joshi and thus unpatentable.

DISCUSSION

A patent claim is anticipated when each and every limitation is expressly or inherently disclosed in a single prior art reference. *Nidec Motor Corp. v. Zhongsgan Broad Ocean Motor Co.*, 851 F.3d 1270, 1273 (Fed. Cir. 2017). Whether a claim is anticipated and what a prior art reference teaches are questions of fact. *In re Chudik*, 851 F.3d 1365, 1371 (Fed. Cir. 2017); *Para-Ordnance Mfg., Inc. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1088 (Fed. Cir. 1995).

This court reviews the Board's determinations on questions of fact for substantial evidence. 5 U.S.C. § 706(2)(E). On review for substantial evidence, this court must sustain the Board's conclusions when they are reasonably drawn from the evidence in record, even if a plausible alternative conclusion could also have been drawn from the evidence.

In re Jolley, 308 F.3d 1317, 1329 (Fed. Cir. 2002). When multiple conclusions can be reasonably drawn from the record, and these conclusions are inconsistent with one another, the "decision to favor one conclusion over the other is the epitome of a decision that must be sustained upon review for substantial evidence." *Id.*

The Board's decision that the '226 patent is anticipated by Joshi is supported by substantial evidence.

Monterey's arguments to the contrary on appeal primarily rely on the contention that Joshi does not disclose "an interface coupled to a multiqueue storage device" because its components DPC 43 and BM 38 cannot together be considered a "multiqueue storage device"—however, the Board reasonably concluded from the evidence on the record that nothing in the claims or specification of the '226 patent indicated that a "multiqueue storage device" must be one physical component and, similarly, that nothing in the patent required any minimum level of access between multiple components to be considered one device. *Id.* at *9–10.

This court refrains from imputing the requirement of a unitary physical structure where the claims and specification do not require one, even when the only preferred embodiment in the claimed invention shows a single physical structure, so long as the specification doesn't otherwise limit the invention to a single component. *Cross Med. Prod., Inc. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1309 (Fed. Cir. 2005); *CCS Fitness v. Brunswick Corp.*, 288 F.3d 1359, 1367 (Fed. Cir. 2002); *Gen. Elec. Co. v. ITC*, 685 F.3d 1034, 1045–46 (Fed. Cir. 2012). The '226 patent's claims and specification do not indicate that a "multiqueue storage device" must be a unitary structure, and in fact the specification makes clear that "[w]hile the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in

form and details may be made without departing from the spirit and scope of the invention." '226 patent, col. 9, ll. 46–50. Therefore, the Board's conclusion that Joshi's disclosure of DPC 43 and BM 38 meets the claim requirements for a "multiqueue storage device" is supported by substantial evidence.

Monterey's only argument that the '226 patent is not anticipated by Joshi that does not rely on the contention that DPC 43 and BM 38 cannot function as a "multiqueue storage device" is that substantial evidence does not support the Board's finding that Joshi's DRDREQS and DRDREQA signals were "address request signals" as described in the '226 patent because an address is not returned in direct response to these signals. Appellant's Br. 21. As the Board explained, this argument also fails because the specification and claims contain no indication that intervening steps between the sending of a signal and the return of an address are prohibited and instead focus on the function of the "address request signals" in ultimately causing the return of an address to facilitate the transfer of data. '226 patent, col 2, ll. 42–59. Monterey's own expert admits that "although it's a very inefficient and distributed method, Joshi claims that it's generating that address" after a sequence of steps initiated by DRDREQS and DRDREQA. Bagherzadeh Dep. 109:18–20, Ex. 1012, IPR2020-01124. Therefore, the Board's conclusion that Joshi's DRDREQS and DRDREQA signals disclose address request signals is supported by substantial evidence.

For the reasons stated above, we hold that the Board's conclusion that the '226 patent is anticipated by Joshi was supported by substantial evidence.

AFFIRMED