

NOTE: This disposition is nonprecedential.

**United States Court of Appeals
for the Federal Circuit**

UNIFICATION TECHNOLOGIES LLC,
Appellant

v.

**MICRON TECHNOLOGY INC., MICRON
SEMICONDUCTOR PRODUCTS, INC., MICRON
TECHNOLOGY TEXAS, LLC, DELL
TECHNOLOGIES INC., DELL, INC., HP INC.,**
Appellees

**DERRICK BRENT, DEPUTY UNDER SECRETARY
OF COMMERCE FOR INTELLECTUAL PROPERTY
AND DEPUTY DIRECTOR OF THE USPTO,**
Intervenor

2023-1348, 2023-1351, 2023-1352

Appeals from the United States Patent and Trademark
Office, Patent Trial and Appeal Board in Nos. IPR2021-
00343, IPR2021-00344, IPR2021-00345.

Decided: August 9, 2024

JONATHAN H. RASTEGAR, Nelson Bumgardner Conroy
PC, Dallas, TX, argued for appellant. Also represented by

EDWARD R. NELSON, III, Fort Worth, TX.

LINDA T. COBERLY, Winston & Strawn LLP, Chicago, IL, argued for appellees. Also represented by LOUIS CAMPBELL, MICHAEL RUECKHEIM, Redwood City, CA; EIMERIC REIG-PLESSIS, San Francisco, CA.

ROBERT J. MCMANUS, Office of the Solicitor, United States Patent and Trademark Office, Alexandria, VA, argued for intervenor. Also represented by PETER J. AYERS, MICHAEL S. FORMAN, FARHEENA YASMEEN RASHEED.

Before CHEN, CUNNINGHAM, and STARK, *Circuit Judges*.

CHEN, *Circuit Judge*.

Unification Technologies LLC (UTL) appeals the Patent Trial and Appeal Board's (Board) final written decisions determining certain challenged claims of U.S. Patent Nos. 8,533,406 ('406 patent) and 8,762,658 ('658 patent) and all challenged claims of U.S. Patent No. 9,632,727 ('727 patent) are unpatentable under 35 U.S.C. § 103. *Micron Tech., Inc. v. Unification Techs. LLC*, No. IPR2021-00343, 2022 WL 22840837 (P.T.A.B. July 8, 2022) ('406 Patent Decision); *Micron Tech., Inc. v. Unification Techs. LLC*, No. IPR2021-00344, 2022 WL 22840770 (P.T.A.B. July 8, 2022) ('658 Patent Decision); *Micron Tech., Inc. v. Unification Techs. LLC*, No. IPR2021-00345, 2022 WL 2784779 (P.T.A.B. July 15, 2022) ('727 Patent Decision). Contrary to UTL's arguments, the Board's decisions did not deprive UTL of due process and the Board did not err in its obviousness analysis. We therefore *affirm* all three decisions.

BACKGROUND

I

In December 2020, Micron Technology Inc., Micron Semiconductor Products, Inc., Micron Technology Texas,

UNIFICATION TECHNOLOGIES LLC v.
MICRON TECHNOLOGY INC.

3

LLC, Dell Technologies Inc., Dell, Inc., and HP Inc. (collectively, Petitioners) filed three petitions requesting *inter partes* review (IPR) of certain claims of the '406, '658, and '727 patents (patents-in-suit). Each petition was signed by Katherine Vidal and listed Ms. Vidal as the lead counsel for Petitioners. In July 2021, the Board instituted IPR on each petition.

A few months after the Board instituted the IPR proceedings, on October 26, 2021, Ms. Vidal was nominated by President Biden for Director of the United States Patent and Trademark Office (Patent Office). Although Ms. Vidal formally continued to represent Petitioners in the IPRs while her nomination was pending, she did not sign Petitioners' reply briefs, nor was her name included in the signature blocks on the reply briefs. On February 10, 2022, after Petitioners filed their reply briefs, Ms. Vidal withdrew as lead counsel from the IPRs. On April 5, 2022, Ms. Vidal was confirmed by the United States Senate as Director of the Patent Office. On April 13, 2022, Ms. Vidal was sworn in as Director. Oral argument in the IPRs was held the same day.

One week after she was sworn in, Director Vidal issued a Memorandum on Recusal Procedures. *See* Patent Office, Director's Memorandum, Procedures for Recusal to Avoid Conflicts of Interest and Delegations of Authority (Apr. 20, 2022), <https://www.uspto.gov/sites/default/files/documents/Director-Memorandum-on-Recusal-Procedures.pdf> (Recusal Memorandum). The Recusal Memorandum set out "the procedures that the [Patent Office] will follow in the event of an actual or potential conflict of interest by the [Director] . . . relating to matters requiring the Director's . . . review, approval, or other involvement." *Id.* at 1.

On May 9, 2022, UTL moved to dismiss the IPRs based on Director Vidal's conflict of interest as a result of her prior representation of Petitioners. The Board denied the motions on June 28, 2022. The Board's order denying the

motions noted that Director Vidal “is recused from these proceedings and took no part in this decision,” citing Director Vidal’s Recusal Memorandum. J.A. 5379. The Board issued its final written decisions in the IPRs on July 8 and 15, 2022, again noting that Director Vidal “is recused from [these] proceeding[s] and took no part in [these] decision[s]” and citing the Recusal Memorandum. *’406 Patent Decision*, 2022 WL 22840837, at n.1; *’658 Patent Decision*, 2022 WL 22840770, at n.1; *’727 Patent Decision*, 2022 WL 2784779, at n.1. UTL subsequently filed requests for Director review of the final written decisions. Because of Director Vidal’s recusal, these requests were referred to, and denied by, the Deputy Director of the Patent Office, Derrick Brent.

II

The patents-in-suit generally relate to managing and deleting data stored in non-volatile memory. *See* *’406 patent* at Abstract; *’658 patent* at Abstract; *’727 patent* at Abstract. The *’406 patent* and the *’727 patent* are each a continuation of the *’658 patent*, and the three patents share similar specifications.

The patents-in-suit identify a problem in the prior art: a disconnect between file systems and data storage devices when data is directed to be erased or deleted. Specifically, the patents describe that:

Typically, when data is no longer useful it may be erased. In many file systems, an erase command deletes a directory entry in the file system while leaving the data in place in the storage device containing the data. Typically, a data storage device is not involved in this type of erase operation.

’406 patent col. 1 ll. 32–36; *’658 patent* col. 1 ll. 29–33; *’727 patent* col. 1 ll. 32–36. In order to address that problem, the patents-in-suit disclose a data storage apparatus that receives an indication or message, indicating that certain

UNIFICATION TECHNOLOGIES LLC v.
MICRON TECHNOLOGY INC.

5

data can be erased. *See, e.g.*, '406 patent col. 2 l. 61 – col. 3 l. 8. In other words, the data storage device is notified of the erase command so that it may take the appropriate action in response.

The parties' disputes concern limitations spanning four independent claims across the patents-in-suit. Claim 15 of the '406 patent recites (emphases added):

15. An apparatus, comprising:

a non-volatile storage medium;

a request receiver module of a storage layer for the non-volatile storage medium configured to receive **an indication that a data structure, corresponding to data stored on the non-volatile storage medium, has been deleted**, wherein the indication comprises a logical identifier that is associated with the data structure by a storage client, and wherein the logical identifier is mapped to a physical address of the data on the non-volatile storage medium; and

a marking module configured to record that the data stored at the physical address mapped to the logical identifier can be erased from the non-volatile storage medium **in response to receiving the indication.**

Claim 1 of the '658 patent is similar, reciting a “message” instead of an “indication” received by the request receiver module, and reciting a “storage module” instead of a “marking module” (emphasis added):

1. An apparatus for managing data stored on a non-volatile storage medium, comprising:

a non-volatile storage medium;

a request receiver module configured to receive a message comprising a logical identifier, **the**

message indicating that data associated with the logical identifier has been erased, wherein the logical identifier is mapped to a physical storage location of the non-volatile storage medium; and

a storage module configured to store persistent data on the non-volatile storage medium in response to the indication, wherein the persistent data is configured to indicate that the data associated with the logical identifier is erased.

Claim 1 of the '727 patent recites (emphases added):

1. An apparatus, comprising:

a solid-state storage medium;

a solid-state storage controller configured to implement storage operations on the solid state storage medium in response to requests from a computer system, including storing data pertaining to logical addresses of a logical address space at respective physical addresses of the solid-state storage medium; and

an indexer, comprised within the solid-state storage controller, **wherein the indexer is configured to assign logical addresses of the logical address space to physical addresses** in use to store data pertaining to the logical addresses on the solid-state storage medium;

wherein the indexer is further configured to remove an assignment between an identified logical address and a physical address of the solid-state storage medium **in response to a message received from a host operating system**, the message indicating that the identified logical address is erased.

Claim 12 of the '727 patent recites (emphases added):

UNIFICATION TECHNOLOGIES LLC v.
MICRON TECHNOLOGY INC.

7

12. A non-volatile solid-state storage system, comprising:

a storage interface configured to communicate with a storage client;

a storage processor coupled to the storage interface;

a flash memory device coupled to the storage processor; and

a logical-to-physical translation layer maintained by the storage processor, wherein the logical-to-physical translation layer maps logical block addresses to corresponding respective physical block addresses of the flash memory device, **wherein the storage processor is configured to:**

receive, from the storage client through the storage interface, an empty-block directive command and a range of logical block addresses,

update the logical-to-physical translation layer to indicate that data stored in physical block addresses corresponding to the received logical block addresses do not need to be preserved, and

store persistent data on the flash memory device, the persistent data indicating that the data corresponding to the received logical block addresses is deleted at the storage client.

The Board's final written decisions found that claims 15–21 and 26 of the '406 patent, claims 1–5 and 8–12 of the '658 patent, and claims 1–6 and 12–16 of the '727 patent (collectively, Challenged Claims) are unpatentable under 35 U.S.C. § 103 over the prior art reference U.S. Patent

No. 7,057,942 (Suda).¹ The Board did not reach Petitioners' alternative grounds for invalidity. Additionally, the Board was unable to ascertain the scope of claims 27–30 of the '406 patent and 22–26 of the '658 patent with reasonable certainty, and accordingly did not reach a decision on the merits for those claims.

UTL timely appealed all three final written decisions to our court. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

STANDARD OF REVIEW

We “review contentions that rights of due process have been violated *de novo*.” *Apple Inc. v. Voip-Pal.com, Inc.*, 976 F.3d 1316, 1323 (Fed. Cir. 2020) (cleaned up).

In an appeal from an IPR decision, we “review the Board’s ultimate obviousness determination *de novo* and its underlying factual findings for substantial evidence.” *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1278 (Fed. Cir. 2017). “A finding is supported by substantial evidence if a reasonable mind might accept the evidence to support the finding.” *Redline Detection, LLC v. Star Envirotech, Inc.*, 811 F.3d 435, 449 (Fed. Cir. 2015) (citations and internal quotation marks omitted).

¹ We note that the Board found dependent claims 4 and 13 of the '727 patent unpatentable over Suda in combination with the prior art reference U.S. Patent No. 7,624,239 (Bennett). However, UTL treats the Board as having found all Challenged Claims unpatentable over Suda alone and makes no argument related to the disclosure of Bennett. *See, e.g.*, Appellant’s Br. 2, 21–23, 30–31.

UNIFICATION TECHNOLOGIES LLC v.
MICRON TECHNOLOGY INC.

9

DISCUSSION

I

UTL argues that Director Vidal’s recusal from the IPRs was insufficient to ensure that it received an impartial adjudication by the Board. Specifically, UTL contends that, as “boss” of the Patent Office and its employees, Director Vidal controls the performance reviews and the existence and quantity of the bonuses of administrative patent judges (APJs), and therefore the APJs who decided the IPRs had a personal pecuniary interest in agreeing with the arguments made by Director Vidal in favor of unpatentability. UTL contends that this violated its right to due process. The remedy that UTL seeks for the alleged due process violation is a total dismissal of the IPRs—for, in its view, Director Vidal’s conflict of interest infects *any* APJ under the Patent Office’s current discretionary compensation structure.² For the reasons explained below, we disagree with UTL that its due process rights were violated.

A party’s right to due process is violated when an adjudicator “has a direct, personal, substantial, pecuniary interest in reaching a conclusion against him in his case.” *Aetna Life Ins. Co. v. Lavoie*, 475 U.S. 813, 821–22 (1986) (quoting *Tumey v. Ohio*, 273 U.S. 510, 523 (1927)). This test does not require us to decide that an adjudicator “in fact . . . was influenced” or possessed “actual bias” due to their pecuniary interest. *Id.* at 825 (citing *In re Murchison*, 349 U.S. 133, 136 (1955)). Rather, we must determine only

² In its reply brief, UTL altered its request for relief to “reverse or vacate and remand,” without explaining how a remand would cure the issue. Reply Br. 5, 32 (emphasis added). In any event, arguments not raised in an opening brief are forfeited. *Stinson v. McDonough*, 92 F.4th 1355, 1362 n.5 (Fed. Cir. 2024).

whether the adjudicator’s direct and substantial interest “would offer a possible temptation to the average . . . [adjudicator] to . . . lead him to not to hold the balance nice, clear and true.” *Id.* at 822 (quoting *Ward v. Village of Monroeville*, 409 U.S. 57, 60 (1972)). Under this test, “a slight pecuniary interest” is insufficient to violate due process, as is an interest that is “highly speculative and contingent.” *Id.* at 825–26.

Here, UTL argues that the APJs who decided the IPRs were conflicted because Director Vidal, in her former capacity as counsel for Petitioners, authored the petitions for IPR and, in her current capacity as Director of the Patent Office, purportedly controls the performance reviews and bonus determinations for all APJs. Appellant’s Br. 24–26; Reply Br. 12–14.³ According to UTL, the APJs would be tempted to agree with the arguments made by their boss,

³ At oral argument, UTL further specified that the alleged problem was that Director Vidal’s name appeared on the petitions for IPR but she waited until *after* Petitioners filed their reply briefs to withdraw, despite being nominated for Director beforehand. Oral Arg. at 6:22–8:11 (available at https://oralarguments.cafc.uscourts.gov/default.aspx?fl=23-1348_06072024.mp3). When pressed on whether its position would effectively require a nominee for Director to immediately withdraw from all proceedings at the Patent Office, UTL conceded that “the prudent course of action would be to not continue to put your name on new filings.” *Id.* at 8:11–8:43. That is precisely what occurred here. Director Vidal’s name was omitted from Petitioners’ reply briefs. See J.A. 4671–4672, 7435, 9579–9580. We therefore view UTL as abandoning its argument that Director Vidal’s withdrawal was “belated” in a way that would influence the APJs’ adjudication of the IPRs. Reply Br. 9.

UNIFICATION TECHNOLOGIES LLC v.
MICRON TECHNOLOGY INC.

11

Director Vidal, in hopes of receiving more favorable bonuses as a result.

UTL's theory fails because it has provided no evidence that the Director controls APJ bonuses or performance reviews. To the contrary, the Patent Office explained at oral argument that its internal operating procedures do not contemplate any involvement by the Director in APJ bonus determinations. Oral Arg. at 25:37–26:05. Further, in a case rejecting a similar due process challenge based on an alleged pecuniary interest of APJs in instituting post-grant proceedings under the America Invents Act (AIA), such as IPRs, in order to earn a bonus, the Patent Office's intervenor brief explained that “APJs are typically reviewed by *Lead APJs*.” Brief for Intervenor at 42, *Mobility Workx, LLC v. Unified Pats., LLC*, 15 F.4th 1146 (Fed. Cir. 2021) (No. 2020-1441), 2020 WL 6710199 (*Mobility Workx* Intervenor Br.) (emphasis added); *Mobility Workx*, 15 F.4th at 1155–56. Our record contains no evidence to the contrary.

UTL's reliance on *United States v. Arthrex, Inc.*, 594 U.S. 1 (2021), is of no help because that case says nothing about the Director controlling APJ bonuses or performance reviews. Nor does 35 U.S.C. § 3(b)(6). That statute merely provides that “[t]he Director may fix the *rate of basic pay* for the administrative patent judges.” 35 U.S.C. § 3(b)(6) (emphasis added). The remaining statutes cited by UTL generally establish other aspects of the Director's responsibilities, such as deciding whether to institute IPR and designating the three-member panel for each IPR, but again do not mention performance reviews or bonuses. *See* 35 U.S.C. §§ 6, 314.

Although the Patent Office's procedures do not foreclose the Director's involvement, UTL has pointed to no evidence of the Director ever inserting herself into the performance evaluation or bonus determination process for a particular APJ. Based on this record, an average APJ—familiar with the Patent Office's standard procedures—

would have no reason to believe that their decision in a particular IPR could affect their bonus determination because of the way that the Director might react if informed of the decision. *See also Mobility Workx*, 15 F.4th at 1156 (“[T]he number of decisional units earned by an APJ ‘is based upon the number of decisions authored’ and ‘does not depend on the outcomes of those decisions.’” (quoting *Mobility Workx* Intervenor Br. 38)). UTL’s theory also depends upon the additional layer of speculation that Director Vidal, among all her responsibilities as Director, would even be aware of the APJs’ decisions in these particular matters.

In *Mobility Workx*, we decided that any financial “interest APJs have” in ruling a certain way in AIA institution decisions to earn a bonus “would be too remote to constitute a due process violation.” 15 F.4th at 1156. Here, too, the APJs’ prospect of receiving a more favorable bonus determination by reaching a particular outcome in the IPRs was highly conditional and speculative at best. This is insufficient to violate due process. *See Aetna*, 475 U.S. at 826–27; *cf. Van Harken v. City of Chicago*, 103 F.3d 1346, 1353 (7th Cir. 1997) (finding hearing officers’ potential fear that letting off too many alleged parking violators might anger and cause their boss, the Director of Revenue, to fire them is a “very indirect, very tenuous stake” insufficient to violate due process).⁴

Thus, UTL has not established that the APJs had an unconstitutional financial interest in deciding the IPRs in

⁴ We also note that the Board’s final written decisions were not decided in a vacuum. The Board held the Challenged Claims unpatentable only after first finding in its institution decisions, *before* Director Vidal was nominated, that Petitioners established a reasonable likelihood of proving the Challenged Claims unpatentable over the same prior art references.

UNIFICATION TECHNOLOGIES LLC v.
MICRON TECHNOLOGY INC.

13

favor of unpatentability, such that its due process rights were violated.

II

UTL next argues that the Board erred by finding the Challenged Claims unpatentable under 35 U.S.C. § 103 over Suda without articulating a motivation to modify Suda or a reasonable expectation of success in modifying Suda. We disagree.

In the ordinary course, a determination of obviousness requires finding “that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted). And “in appropriate circumstances, a patent can be obvious in light of a single prior art reference if it would have been obvious to modify that reference to arrive at the patented invention.” *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016).

In *Realtime Data, LLC v. Iancu*, 912 F.3d 1368 (Fed. Cir. 2019), however, we addressed the scenario in which a claim is rendered unpatentable under 35 U.S.C. § 103 based on a single prior art reference that discloses every claim limitation. There, the Board agreed with the IPR petitioner’s argument that a single reference, O’Brien, taught every limitation of the claims at issue and that a second reference, Nelson, demonstrated how a skilled artisan would have understood the disclosure of O’Brien, such that the claims were unpatentable under 35 U.S.C. § 103. *Id.* at 1372–73. We concluded that the Board was free to find, in the context of an obviousness analysis, that “O’Brien alone disclosed every element of [the] claims,” and “because the Board did not rely on Nelson for the disclosure of a particular element or teaching, the Board had no obligation to

find a motivation to combine O'Brien and Nelson." *Id.* at 1373.

UTL contends that *Realtime Data* is inapplicable to the instant case because the Board relied on the opinions of Petitioners' expert, Dr. Baker, to supply missing limitations not found in Suda. UTL misinterprets the Board's reliance on Dr. Baker's testimony. The Board relied on Dr. Baker not to supply limitations missing from Suda, but to inform the Board's analysis as to how a skilled artisan would have understood Suda's disclosure. For example, in the Board's discussion of the "indication" limitation in claim 15 of the '406 patent and the "message" limitation in claim 1 of the '658 patent, the Board credited "Dr. Baker's analysis . . . as to how an ordinarily skilled artisan *would have understood Suda's description* of an 'erase command' sent by the digital camera." *'406 Patent Decision*, 2022 WL 22840837, at *13 (emphasis added); *'658 Patent Decision*, 2022 WL 22840770, at *13 (emphasis added). The Board's analysis comports with the IPR petitions, each of which presented, as a distinct ground for invalidity, obviousness based on Suda, as understood by a skilled artisan, teaching every limitation of the Challenged Claims. *See* J.A. 249–270, 5525–5544, 7981–8002.

The Board thus found the Challenged Claims unpatentable under 35 U.S.C. § 103 in light of a single prior art reference, Suda, which the Board found taught every limitation.⁵ Because no modification to Suda was necessary to arrive at the claimed invention, the Board was "not

⁵ For claims 4 and 13 of the '727 patent, the Board did find a motivation to combine Suda with Bennett. *See supra* note 1; *'727 Patent Decision*, 2022 WL 2784779, at *21–22. UTL does not dispute this finding or otherwise separately argue the patentability of these claims.

UNIFICATION TECHNOLOGIES LLC v.
MICRON TECHNOLOGY INC.

15

required to make any finding regarding a motivation to” modify Suda. *Realtime Data*, 912 F.3d at 1373.

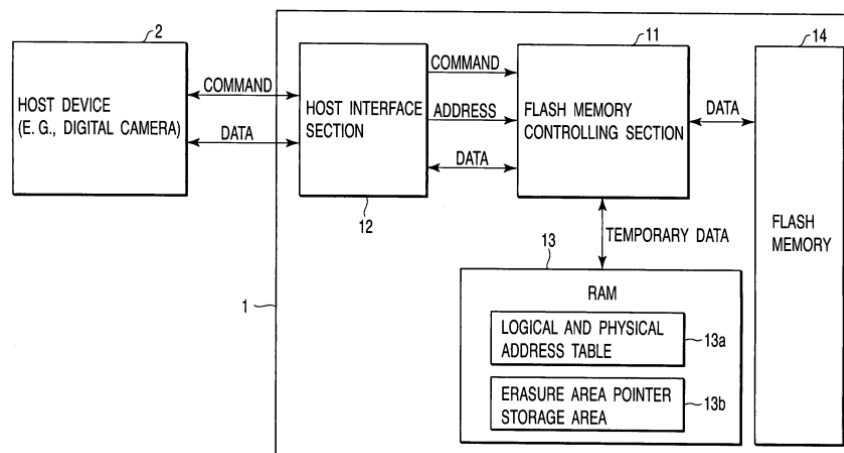
Accordingly, the Board did not err by concluding that Suda renders the Challenged Claims unpatentable under 35 U.S.C. § 103 without finding a motivation to modify Suda with a reasonable expectation of success.

III

Finally, we turn to UTL’s argument that the Board erred in finding that Suda discloses certain limitations of the Challenged Claims. Because the Board’s findings are supported by substantial evidence, we affirm its decisions.

A. Suda

Suda discloses “a memory management device for managing a nonvolatile semiconductor memory[,] which comprises a plurality of blocks, and permits data to be erased in units of one block.” Suda col. 1 ll. 60–63. Figure 1 of Suda, reproduced below, displays “a block diagram of an example of the structure of a memory card (memory device) 1 according to the embodiment of the present invention”:



Id. col. 2 ll. 19–21, FIG. 1. In Figure 1, host device 2, such as a digital camera, is connected to memory card 1, which

comprises host interface section 12, flash memory controlling section 11, and flash memory 14. *Id.* col. 2 ll. 61–65.

Suda explains that when the host device 2 issues an erase command, “the flash memory controlling section 11 refers to the logical and physical address table 13a, and detects the physical address of a physical block related to a logical block given an address design[at]ed in the erasure command.” *Id.* col. 7 ll. 30–34. The flash memory controlling section 11 then “determines whether an address range corresponding to an area in which the data items to be erased in response to the erase command are stored is already stored in the erasure area pointer storage area 13b.” *Id.* col. 7 ll. 38–42. If not, “the flash memory controlling section 11 performs rewriting processing to change data written to the erasure area pointer storage area 13b” so that the relevant area is “set as the virtual erasure area.” *Id.* col. 7 ll. 43–51. Suda discloses that through this process of writing erasure area pointers in response to an erase command, the time for erasing data is shortened. *Id.* col. 5 ll. 9–13.

B. The “Indication” and “Message” Limitations

Independent claim 15 of the ’406 patent recites “an indication that a data structure, corresponding to data stored on the non-volatile storage medium, has been deleted.” Independent claim 1 of the ’658 patent similarly recites a “message indicating that data associated with the logical identifier has been erased.” The Board found that Suda’s “erase command” teaches these limitations. *’406 Patent Decision*, 2022 WL 22840837, at *11–14; *’658 Patent Decision*, 2022 WL 22840770, at *11–13.

UTL argues that these limitations are not satisfied by Suda’s erase command because the erase command “does not indicate that data has been deleted/erased at the file system level.” Appellant’s Br. 38. In other words, UTL argues that “[t]he claims require an indication that data *has been deleted/erased at the file system level*,” and no such

UNIFICATION TECHNOLOGIES LLC v.
MICRON TECHNOLOGY INC.

17

deletion/erasure has taken place when Suda's erase command is issued. *Id.* at 39 (emphases added).

Substantial evidence supports the Board's findings that these limitations are met by the "erase command." The Board found that Suda's digital camera "issues an erase command to erase particular pages of data stored in the flash memory." '406 *Patent Decision*, 2022 WL 22840837, at *12 (citing Suda col. 7 ll. 11–19, col. 8 l. 66 – col. 9 l. 3); '658 *Patent Decision*, 2022 WL 22840770, at *12 (same). The Board relied on Petitioners' expert, Dr. Baker, for "how an ordinarily skilled artisan would have understood Suda's description of an 'erase command' sent by the digital camera." '406 *Patent Decision*, 2022 WL 22840837, at *12–13; '658 *Patent Decision*, 2022 WL 22840770, at *12–13. The Board also found that Dr. Baker's explanation is consistent with the '406 patent and the '658 patent's description of the prior art in the Background of the Invention section, which states that "[t]ypically, when data is no longer useful it may be erased. In many file systems, *an erase command deletes a directory entry in the file system while leaving the data in place in the storage device containing the data.*" '406 *Patent Decision*, 2022 WL 22840837, at *13 (emphasis added) (quoting '406 patent col. 1 ll. 32–35); '658 *Patent Decision*, 2022 WL 22840770, at *13 (emphasis added) (quoting '658 patent col. 1 ll. 29–32).

Ultimately, the Board concluded that a skilled artisan would understand that when Suda's erase command is issued, an entry has been deleted at the file system level. The Board's analysis is supported by substantial evidence.

C. The "Marking Module" Limitation

Claim 15 of the '406 patent recites "a request receiver module . . . configured to receive an indication that a data structure . . . has been deleted," and "a marking module configured to record that the data stored at the physical address mapped to the logical identifier can be

erased . . . in response to receiving the indication.” The Board found that Suda’s host interface section 12 is the claimed “request receiver module” and that Suda’s flash memory controlling section 11 is the claimed “marking module.” *’406 Patent Decision*, 2022 WL 22840837, at *10–11.

UTL argues that flash memory controlling section 11 cannot be the claimed marking module because Suda describes that the host interface section 12 extracts “address information” from the erase command issued by the host device 2, and therefore sends what UTL terms a “backend instruction command” to flash memory controlling section 11. Appellant’s Br. 41–42. According to UTL, because flash memory controlling section 11 acts in response to the backend instruction command, rather than the erase command, it does not meet the claim’s requirement that the marking module act “in response to receiving the indication.” UTL also takes issue with the Board’s finding that “[c]laim 15 does not recite that the marking module itself receives the indication.” *’406 Patent Decision*, 2022 WL 22840837, at *10.

We disagree with UTL. At oral argument, UTL disclaimed that it was presenting to us an issue of claim construction. Oral Arg. at 10:58–12:28. Accordingly, under the plain and ordinary meaning of the term “marking module,” the Board reasonably found that flash memory controlling section 11 acts in response to receiving the claimed indication. *See ’406 Patent Decision*, 2022 WL 22840837, at *5–6, *10. The Board cited five separate statements in Suda describing that the flash memory controlling section 11 acts “in response to” the erase command. *See id.* at *10; *see, e.g.*, Suda col. 5, ll. 38–43 (“The flash memory controlling section 11 designates as a start pointer a page address . . . *in response to* an erase command from the host device 2.” (emphasis added)). Given those express disclosures, the Board reasonably disagreed with UTL “that flash memory controlling section 11 records data in

UNIFICATION TECHNOLOGIES LLC v.
MICRON TECHNOLOGY INC.

19

response to the [b]ackend [instruction] [c]ommand rather than the Initial Message (i.e., the erase command).” ’406 *Patent Decision*, 2022 WL 22840837, at *10. Substantial evidence supports the Board’s findings as to this limitation.

D. The “Indexer” Limitation

Independent claim 1 of the ’727 patent recites “an indexer . . . configured to assign logical addresses . . . to physical addresses.” The Board found that Suda’s flash memory controlling section 11 satisfies this requirement of the claimed indexer. ’727 *Patent Decision*, 2022 WL 2784779, at *9–10. Specifically, the Board found that flash memory controlling section 11 “creates and removes the assignments” between logical and physical addresses, using table 13a to store the data indicating such relationships. *Id.* at *10.

UTL argues that Suda’s table 13a merely stores a *relationship* between logical and physical addresses, not an assignment. Appellant’s Br. 45. Even if table 13a did show an assignment, UTL contends that Suda does not identify flash memory controlling section 11 as the component that performs the assignment. *Id.* at 45–46.

We find that substantial evidence supports the Board’s conclusions. The Board noted that table 13a in Figure 7 of Suda “appears to show an assignment of logical addresses (0X40000–0X60000) to physical addresses (blocks 3–5).” ’727 *Patent Decision*, 2022 WL 2784779, at *10 (citing Suda col. 7 ll. 14–17, FIG. 7). The Board cited to evidence that Suda’s flash memory controlling section 11 “manages” table 13a, “cancel[s]” the relations between logical addresses and physical addresses in table 13a, and “control[s]” the relations of physical block addresses to logical block addresses. *See id.* at *9–10; Suda col. 3 ll. 13–15, 64–67, col. 5 l. 62 – col. 6 l. 3. From this, the Board reasonably concluded that flash memory controlling section 11 performs the assignment of logical addresses to physical addresses recorded in table 13a.

UTL also cites a single statement in Suda that supports its own position, namely, that it is table 13a itself that “manages logical address and physical addresses.” Reply Br. 26 (quoting Suda col. 3 ll. 43–47). This lone statement, however, is not sufficient to render the Board’s decision unsupported by substantial evidence. *See Redline Detection, LLC v. Star Envirotech, Inc.*, 811 F.3d 435, 449 (Fed. Cir. 2015) (“If the evidence in the record will support several reasonable but contradictory conclusions, we will not find the Board’s decision unsupported by substantial evidence simply because the Board chose one conclusion over another plausible alternative.” (cleaned up)).

Accordingly, we find that the Board’s conclusion that Suda teaches this limitation is supported by substantial evidence.

CONCLUSION

We have considered UTL’s remaining arguments, including as to the remaining limitations challenged by UTL, and find them unpersuasive. For the foregoing reasons, we *affirm* the Board’s final written decisions.

AFFIRMED