NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

INTEL CORPORATION,
Appellant

v.

PACT XPP SCHWEIZ AG,
Appellee

2023-1537

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2020-00535.

Decided: December 11, 2024

JOHN C. O'QUINN, Kirkland & Ellis LLP, Washington, DC, argued for appellant. Also represented by DIVA R. HOLLIS; ROBERT ALAN APPLEBY, JAMES E. MARINA, New York, NY.

SANFORD IAN WEISBURST, Quinn Emanuel Urquhart & Sullivan, LLP, New York, NY, argued for appellee. Also represented by RON HAGIZ; NIMA HEFAZI, FREDERICK A. LORIG, Los Angeles, CA; MARK YEH-KAI TUNG, Redwood Shores, CA.

Before MOORE, *Chief Judge*, TARANTO, *Circuit Judge*, and SCHROEDER, *District Judge*.[1]

MOORE, *Chief Judge*.

Intel Corporation (Intel) appeals an *inter partes* review final written decision from the Patent Trial and Appeal Board (Board) holding that Intel failed to prove claim 8 and claims which depend from claim 8 of U.S. Patent No. 8,312,301 would have been obvious. We affirm.

BACKGROUND

PACT XPP Schweiz AG (PACT) owns the '301 patent, which discloses a multiprocessor system where different data processing components can be operated at reduced clock frequencies (i.e., processor speed) to save power when the battery level is low. '301 patent at 1:21–22, 2:20–40, 7:48–53, 10:49–58. Claim 8 is representative:

> 8. A processor device, comprising:
>
> a plurality of data processing elements adapted for programmably processing sequences and to which tasks are assigned, each of the data processing elements having at least one Arithmetic Logic Unit; and
>
> at least one bus system at least one of (a) interconnecting at least some of the data processing elements and (b) connecting at least some of the data processing elements with at least one of peripherals and external memory;
>
> wherein:

[1] Honorable Robert W. Schroeder, III, District Judge, United States District Court for the Eastern District of Texas, sitting by designation.

> each of at least some of the data processing elements is capable of operating at a clock frequency different than at least one other of the data processing elements; and
>
> the processor device is adapted for *reducing clock frequencies of the data processing elements in response to a determination that a power reserve of a battery is below a predetermined threshold*.

'301 patent at 15:59–16:9 (emphasis added).

Intel challenged claims 3, 6–10, 12–19, 23–26, 30, 32, 35, and 36 of the '301 patent as obvious over the combination of U.S. Patent Nos. 6,141,762 (Nicol) and 6,535,798 (Bhatia). The Board held independent claims 3, 6, 10, 12, 23, and 24 and dependent claim 7 were unpatentable in view of Nicol alone or in combination with Bhatia, but independent claim 8 and claims which depend from claim 8 (claims 9, 13–19, 25, 26, 30, 32, 35, and 36) were not unpatentable. Intel appeals the Board's determination with respect to claim 8 and its dependents. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

Obviousness is a question of law based on underlying findings of fact. *Regents of Univ. of Cal. v. Broad Inst., Inc.*, 903 F.3d 1286, 1291 (Fed. Cir. 2018). We review the Board's ultimate conclusion of obviousness de novo and its underlying factual findings for substantial evidence. *Id.*

Intel argues the Board legally erred by refusing to consider U.S. Patent No. 6,704,877 (Cline) as background knowledge a skilled artisan would have in evaluating Nicol and Bhatia's teachings. Appellant's Br. 30–37. We do not agree. In determining claim 8 would not have been obvious, the Board found "no teaching or suggestion in either Nicol or Bhatia of determining the power reserve of a battery, let alone reducing clock frequencies in response to a

determination that the power reserve is below a predetermined threshold." J.A. 52. The Board found Intel relied on Cline to supply a missing claim limitation—reducing clock frequency in response to "detection of a low battery condition"—not taught by either Nicol or Bhatia, rather than, as Intel argued, to describe the state of the art. J.A. 53–54. Thus, Intel needed to include Cline in the asserted grounds of unpatentability set forth in its petition and persuasively show a skilled artisan would have been motivated to combine Cline with Nicol and Bhatia. J.A. 53. Because Intel failed to do so, the Board refused to consider Cline.

Intel frames this as legal error, but the "level of skill in the art and the scope and content of the prior art are fact questions we review for substantial evidence." *Neptune Generics, LLC v. Eli Lilly & Co.*, 921 F.3d 1372, 1377 (Fed. Cir. 2019); *see also Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 992 (Fed. Cir. 2017) (listing "[skilled] artisans' background knowledge" as a fact finding). We see no error in the Board's treatment of Cline. Substantial evidence supports the Board's finding that neither Bhatia nor Nicol discloses the claim limitation. J.A. 52, 54–55; Oral Arg. at 4:40–54, 6:32–46, https://oralarguments.cafc.uscourts.gov/default.aspx?fl=23-1537_12032024.mp3. Under substantial evidence review, we cannot overturn the Board's finding that Cline is used to supply a missing claim limitation, and not as evidence of a skilled artisan's background knowledge. *Falko-Gunter Falkner v. Inglis*, 448 F.3d 1357, 1364 (Fed. Cir. 2006) ("An agency decision can be supported by substantial evidence, even where the record will support several reasonable but contradictory conclusions.").

Intel also argues the Board legally erred by refusing to consider the *Advanced Configuration and Power Interface* specification (ACPI) as background knowledge a skilled artisan would have in evaluating Bhatia's teachings. Appellant's Br. 37–44. We do not agree. As a preliminary matter, the Board rejected Intel's argument that "Bhatia

incorporates the entirety of the ACPI specification by its reference to processor power management states disclosed therein." J.A. 57–58. Intel makes the same argument to this court. Appellant's Br. 16, 19, 37, 44. There is simply no merit to this argument. The Board found that while Intel had, in its petition, identified certain portions of the ACPI with regard to certain grounds, the arguments it made in reply differed from the arguments made in the petition. J.A. 57. Thus, the Board found them untimely. In its petition, Intel did not even cite ACPI when discussing claim 8. *See* J.A. 257–62. In its reply, Intel cited ACPI § 3.4 (Controlling Device Power) and § 3.8 (Battery Management). J.A. 573 (citing J.A. 3285); J.A. 574–75 (citing J.A. 3291–92). "The Board's determinations that a party exceeded the scope of a proper reply are reviewed for abuse of discretion." *Apple Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697, 705 (Fed. Cir. 2020). We see no abuse of discretion. The Board found Bhatia does not incorporate the relevant ACPI sections by reference that Intel cited in reply, let alone the entirety of ACPI. J.A. 57–58.

Bhatia references ACPI's processor power states (C0–C3) and "an interrupt defined by the ACPI specification." *E.g.*, J.A. 2360 at 12:58–61; J.A. 2361 at 13:33. Processor power states are described in ACPI §§ 2.5, 3.5, and 8. J.A. 3278, 3288, 3408. Interrupts are described in ACPI §§ 3.4 and 3.5. J.A. 3285, 3288. However, given Bhatia's references to processor power states in § 3.5, the Board found Bhatia's reference to "interrupt" is not directed to § 3.4. J.A. 56–57. By contrast, in its reply, Intel cited ACPI's device power states (D0–D3) and battery management, described in ACPI §§ 3.4 and 3.8, respectively. J.A. 573–75 (citing J.A. 3285, 3291–92). Substantial evidence supports the Board's finding that Bhatia does not reference ACPI in the context of device power management (ACPI § 3.4) and battery management (ACPI § 3.8). J.A. 57.

CONCLUSION

We have considered Intel's remaining arguments and find them unpersuasive. We affirm the Board's determination that Intel failed to prove claim 8 and claims which depend from claim 8 of the '301 patent would have been obvious.

AFFIRMED