NOTE: This disposition is nonprecedential.

United States Court of Appeals for the Federal Circuit

VIASAT, INC.,
Appellant

v.

WESTERN DIGITAL TECHNOLOGIES, INC.,
Appellee

2024-1483

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board in No. IPR2022-01171.

Decided: January 7, 2026

MATTHEW R. FORD, Bartlit Beck LLP, Chicago, IL, argued for appellant. Also represented by MEG E. FASULO, NEVIN M. GEWERTZ, JOHN SCOTT MCBRIDE, RAVI SHAH; NOSSON KNOBLOCH, Denver, CO; DAVID ZIMMER, Zimmer, Citron & Clarke LLP, Cambridge, MA.

BRIAN M. BUROKER, Gibson Dunn & Crutcher, LLP, Washington, DC, argued for appellee. Also represented by NATHAN ROBERT CURTIS, Dallas, TX; L. KIERAN KIECKHEFER, San Francisco, CA.

Before CHEN, BRYSON, and CUNNINGHAM, *Circuit Judges*.

BRYSON, *Circuit Judge*.

In this appeal from a final written decision of the Patent Trial and Appeal Board, the patentee, Viasat, Inc., ("Viasat") challenges the Board's decision that certain claims of Viasat's patent-in-suit are unpatentable for obviousness. We hold that substantial evidence supports the Board's obviousness decision, and we therefore affirm.

I

Viasat is the owner of U.S. Patent No. 8,966,347 ("the '347 patent"), titled "Forward Error Correction with Parallel Error Detection for Flash Memories." The patent is directed to methods and systems for error correction in data retrieved from flash memory. Because flash memory is prone to an increasing error rate in the data over time, the invention is designed to modify the error correction process to make it more robust as the number of errors in the stored data begins to climb.

One method for correcting errors in flash memory data is to use a technique referred to as forward error correction ("FEC"), which generally uses an error correction code ("ECC") to generate and store redundant information alongside the original data. When the original data is retrieved from memory, it is compared against the redundant information, which enables the system to detect and ultimately correct the corrupted data.

System claims 13 through 23 of the '347 patent are at issue in this case.[1] Independent claim 13 is representative. It reads as follows:

13. A system comprising:

[a] an encoder to encode data using forward error correction coding;

[b] a flash memory to store the encoded data;

[c] a decoder to retrieve the encoded data stored in the flash memory to generate a data stream, and [d] to process the data stream to correct errors in the data stream associated with the flash memory using at least a first error correction sub-module; and

[e] a controller to:

monitor a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory;

[f] determine that the monitored metric exceeds a threshold;

[g] in response to the determination, modify the forward error correction coding for use by the encoder in subsequently encoding data for storage in the flash memory; and

[h] in response to the determination, powering-up, from an inactive mode, a second error correction submodule arranged in parallel with the first error

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[1] The PTAB also found method claims 1–11 to be unpatentable, but Viasat has not appealed the PTAB's decision with respect to those claims.

> correction sub-module for subsequent data stream processing.[2]

'347 patent, col. 11, line 40, through col. 12, line 10.

For present purposes, the critical portions of claim 13 are limitations 13[c] and 13[d], which describe the function of the decoder as being "to retrieve the encoded data stored in the flash memory to generate a data stream, and to process the data stream to correct errors in the data stream associated with the flash memory using at least a first error correction sub-module." *Id.*, col. 11, ll. 44–48.

II

Western Digital Technologies, Inc., ("Western Digital") filed a petition for *inter partes* review of claims 1 through 11 and 13 through 23 of the '347 patent. The Patent Trial and Appeal Board granted the petition, and in its final written decision the Board found all the challenged claims to be unpatentable for obviousness. J.A. 1. In so finding, the Board relied on prior art published patent applications to Diggs and Cheng.[3] While the Board relied on combinations of Diggs and Cheng for the disclosure of certain limitations, its decision found that the 13[c] and 13[d] limitations at issue on appeal were disclosed by Diggs alone, and thus only Diggs is relevant to our analysis here. J.A. 29–32.

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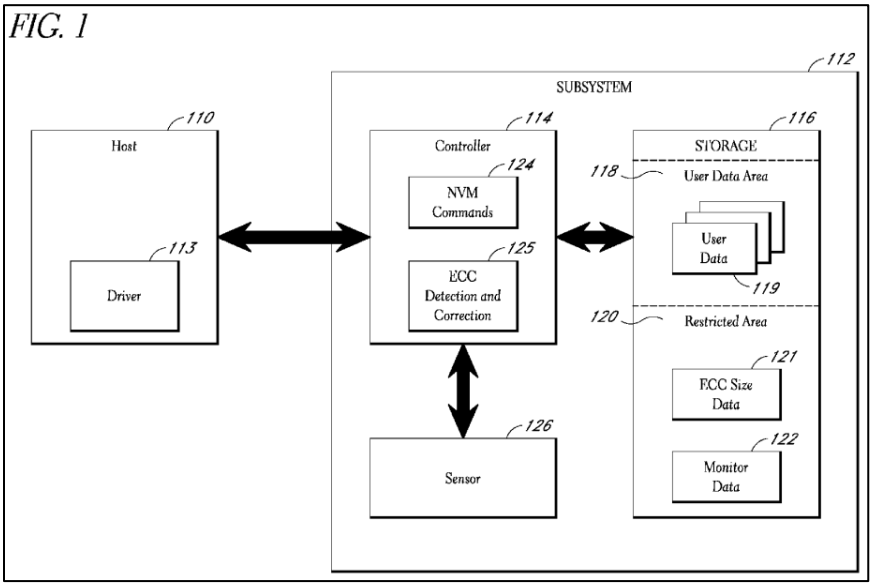
[2] In its briefing before the Board, Western Digital added the bracketed letters to the claims to facilitate analysis, and Viasat relied on these same letter assignments in its appellate brief. The claims are reproduced here including the bracketed letters employed by the parties and the Board.

[3] The Diggs reference is Pub. No. US 2009/0070651; the Cheng reference is Pub. No. US 2009/0276570.

Diggs is directed to a system for adjustable error correction in solid-state storage systems, such as flash memory storage. Diggs ¶¶ 2, 4, 7–8, J.A. 451. The Diggs system is very similar to the invention recited in the '347 patent, in that the Diggs system, like the patented system, uses a controller and a decoding device to retrieve signals from the solid-state memory, to decode those signals, and to detect and correct the errors in the data revealed by the error correction mechanism.

In the portion of its decision pertinent to the issue presented in this appeal, the Board addressed Western Digital's argument that the "decoder" recited in claim 13 of the '347 patent is disclosed by the Diggs Controller. The Board noted that figure 1 of Diggs, which depicts an embodiment of the Diggs invention, shows that Diggs contains a Controller, designated as component 114. The Controller incorporates the ECC Detection and Correction module, which is designated as component 125. Diggs ¶ 23, J.A. 452. Figure 1 of Diggs, J.A. 447, is depicted below.



In the proceedings before the Board, the parties focused on whether Diggs teaches a "decoder" that both "retrieve[s] the encoded data stored in the flash memory to generate a data stream," as recited in claim element 13[c] of the '347 patent, and also "process[es] the data stream to correct errors in the data stream," as recited in claim element 13[d] of the patent.

The parties agreed that the component denominated "Controller" in Diggs (component 114) performs the function of retrieving the encoded data to generate a data stream, and that the component denominated "ECC Detection and Correction" in Diggs (component 125) performs the function of processing the data stream to correct errors. J.A. 30–31. The parties disagreed, however, about whether that meant that the component in Diggs that performs the retrieval function is separate from the component that performs the error correction function.

Viasat argued that because the retrieval function in Diggs is performed by the Diggs Controller, and the correction function in Diggs is performed by the ECC Detection and Correction component, the two functions are not performed by a single decoder, but are performed by different components. Western Digital responded that in Diggs the ECC Detection and Correction module (125) is part of the Controller (114) and thus the same component performs the functions of data retrieval and correction.

The Board noted that it was undisputed that Diggs's ECC Detection and Correction module (125) is incorporated within the Diggs Controller (114). J.A. 31. For that reason, the Board found that the Diggs Controller, including the incorporated ECC Detection and Correction module, performs the two related functions of the "decoder," as set forth in claim 13[c] of the '347 patent.

The Board explained that although the ECC module in Diggs "handles the decoding, and another portion of

controller 114 handles data retrieval, this division of labor is not inconsistent with claim 13, which does not require that the functions of a decoder reside within one circuit." J.A. 31. Accordingly, despite the difference in terminology between Diggs and claim 13 of the '347 patent, the Board found that "the structure disclosed by Diggs fits comfortably within the structure defined by claim 13," *id.,* and that Diggs therefore discloses circuitry that performs both the tasks of retrieving data from the flash memory and processing that data to correct errors.

Based on that analysis, the Board found that the difference between the relevant portions of the structures described in Diggs and in claim 13 was a "semantic discrepanc[y]" rather than a difference in substance. J.A. 31–32 (internal citation omitted). The Board therefore concluded that Western Digital had shown that claim 13 of the '347 patent was unpatentable for obviousness. Based on that conclusion and its analysis of the other claims before it, the Board found that claims 1 through 11 and claims 13 through 23 would have been obvious in light of the combination of Diggs and Cheng.

Viasat appealed to this court, focusing entirely on the Board's analysis of the patentability of claim 13.[4]

III

Viasat's argument on appeal is simple: Viasat contends that claim 13 of the '347 patent requires that the "decoder" both "retrieve the encoded data" and "correct errors." Appellant's Br. 1. In Diggs, according to Viasat,

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[4] Viasat has not challenged the Board's finding that limitation 13[h] is taught by Cheng and that, subject to the dispute over limitations 13[c] and [d], claims 1–11 and 14–23 are rendered obvious by the combination of Diggs and Cheng.

the Controller retrieves the encoded data, while the decoder (the ECC Detection and Correction module, according to Viasat) is "presented with the data already retrieved from flash by the controller." *Id.* at 2. Viasat argues that the controller of claim 13 does not retrieve the data stream from the flash memory, but simply monitors the error rate and activates the additional error correction feature if and when needed. *Id.* According to Viasat, the difference in the respective roles of those two components in Diggs and in the device recited in claim 13 constitutes a fundamental structural distinction between the architecture of Diggs and the architecture of claim 13. In view of that difference, Viasat argues, the Board erred in finding that the limitations in claim elements 13[c] and [d] were disclosed by Diggs.

Viasat's argument is not persuasive. As shown in figure 1 of Diggs, the decoding mechanism in Diggs–the ECC Detection and Correction module (125)—is part of the Diggs Controller (114). For that reason, the Board found that the Controller in Diggs both receives the data stream and processes it, thus performing all the functions of the decoder recited in claim 13. J.A. 30–31.

The parties disagree about whether the Board's decision was based on a finding of fact or on an implicit claim construction. Viasat argues that claim 13 should be construed to require that the functions of the controller and the decoder be performed by separate entities, and that the Board implicitly rejected that claim construction. Western Digital, on the other hand, interprets the Board's decision as turning on a finding of fact—that the Diggs Controller performs all the functions assigned by claim 13 to the decoder. Either interpretation would lead to the same conclusion, but we interpret the Board's ruling as principally based on a factual finding, and we therefore review the Board's decision for substantial evidence.

1. To begin with, it is undisputed that the Diggs Controller receives the encoded data to generate a data stream. In addition, it is clear that Diggs's ECC Detection and Correction module, which processes the data stream to correct errors, is part of the Diggs Controller. Thus, the Board was justified in finding that the functions of receiving the data stream from the flash memory and processing that data stream to make corrections are both performed by the Diggs Controller, even though in Diggs the latter function is performed by a sub-module of the Controller.

According to Viasat, the difference between Diggs and the invention recited in claim 13 of the '347 patent is that in Diggs the ECC Detection and Correction structure performs one of the functions of the decoder of claim 13 (processing the data stream to correct errors in the data stream) but does not perform the other designated function of the decoder (retrieving data from the flash memory to generate a data stream). In Diggs, Viasat argues, that function is performed not by the decoder (the ECC Detection and Correction module), but by the Controller.

As the Board found, that distinction is inconsequential. Figure 1 of Diggs shows that the ECC Detection and Correction module (125) in Diggs is part of the Controller (114), and the text of the Diggs reference confirms that the "controller 114 further includes an ECC detection and correction module 125." Diggs ¶ 23, J.A. 452. The two functions that the '347 patent assigns to the decoder are thus performed by the Controller in Diggs through the incorporated ECC Detection and Correction module. The Board therefore properly rejected Viasat's core argument for distinguishing Diggs—that a single entity in Diggs does not perform both the retrieval function and the processing function. Accordingly, we reject Viasat's argument, which the Board properly characterized as reducing to one of nomenclature.

2. We would reach the same result in this case if we viewed the Board as having based its decision on an implicit construction of claim 13, to wit, as not requiring that the decoder and controller consist of physically separate circuitry. The claim language does not compel us to interpret claim 13 in that fashion, and in fact the specification of the '347 patent suggests the opposite.

The specification teaches that the encoder, decoder, and controller "may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits." '347 patent, col. 3, ll. 34–40. That language indicates that the claim language, properly construed, provides that the functions of the decoder and the controller of claim 13 can be performed by varying sets of circuits, individually or collectively. In other words, they can be performed by the same structure.

In arguing to the contrary, Viasat relies on two cases involving mechanical patents in which the claims recited inventions having distinct components. In the first, *Becton, Dickinson & Co. v. Tyco Healthcare Group*, 616 F.3d 1249 (Fed. Cir. 2010), the court wrote that when a claim lists elements separately, "the clear implication of the claim language is that those elements are distinct components of the patented invention." *Id.* at 1254 (citation modified). In the second, *Kyocera Senco Industrial Tools Inc. v. International Trade Commission*, 22 F.4th 1369 (Fed. Cir. 2022), the court similarly explained that when a patent claim separately lists two mechanical components, it is presumed that those components are distinct. *Id.* at 1382.

That presumption has force with regard to mechanical patents, in which particular functions are typically

performed by physically discrete components. It is less clearly applicable to electronic patents in which particular functions are frequently performed by combinations of circuitry that are not necessarily contained in segregated physical packages. What ultimately matters in this case is whether the patent at issue indicates that the claimed functions may be performed by a shared structure. *See Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1231–32 (Fed. Cir. 2011); *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1304 (Fed. Cir. 2011); *NTP Inc. v. Research in Motion*, 418 F.3d 1282, 1310 (Fed. Cir. 2005).

That point is illustrated by this court's decision in *Linear Technology Corp. v. International Trade Commission*, 566 F.3d 1049 (Fed. Cir. 2009). That case involved claims of an electronic patent that recited a "second circuit" and a "third circuit" that performed particular functions. The International Trade Commission construed those limitations not to require the two circuits to be entirely distinct, without common circuit elements. Instead, the Commission construed the claim language to require only that the two circuits perform their stated functions.

This court agreed with the Commission's construction of the terms "second circuit" and "third circuit," holding the two terms "to not require entirely separate and distinct circuits." 566 F.3d at 1055. The court explained that

> there is nothing in the claim language or specification that supports narrowly construing the terms to require a specific structural requirement or entirely distinct "second" and "third" circuits. Rather, the "second" and "third" circuits must only perform their stated functions. For example, what is required is that the "second circuit" "generate[es] a first control signal . . . to vary the duty cycle," not that any particular components make up this circuit. In fact, the '258 patent's specification

> expressly discloses that the "second circuit" and "third circuit" can share common components. For example, figure 2 shows that components of the "second circuit"—such as the reference circuit 37—can also be part of the "third circuit."

Id.

The same analysis applies in this case. While there is overlap in the Diggs circuitry that performs the functions of the controller and the decoder of the '347 patent, nothing in the '347 patent suggests that such overlap is impermissible. In fact, as noted above, the specification of the '347 patent makes it clear that the components of the systems claimed in the patent—particularly the encoder, the decoder, and the controller—may be implemented by various circuits that individually or collectively are "adapted to perform some or all of the applicable functions in hardware." '347 patent, col. 3, ll. 33–40. *See also id.*, col. 5, line 64, though col. 6, line 3 ("These components and sub-modules" may be implemented with circuits "adapted to perform some or all the applicable functions in hardware. Alternatively, the functions may be performed by one or more processing units (or cores), on one or more integrated circuits."). The specification of the '347 patent thus makes it clear that under the proper construction of claim 13, the identity of the particular module or sub-module that performs each task is not critical.

We agree with the Board that the Diggs reference maps to the structures and functions set forth in claim elements 13[c] and [d] of the '347 patent, and we therefore uphold the Board's decision that the combination of Diggs and Cheng rendered claim 13 unpatentable for obviousness.

AFFIRMED